


SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

System Block Diagram

 Apple Inc.

DRAWING NUMBER
051-9589

REVISION
4.18.0

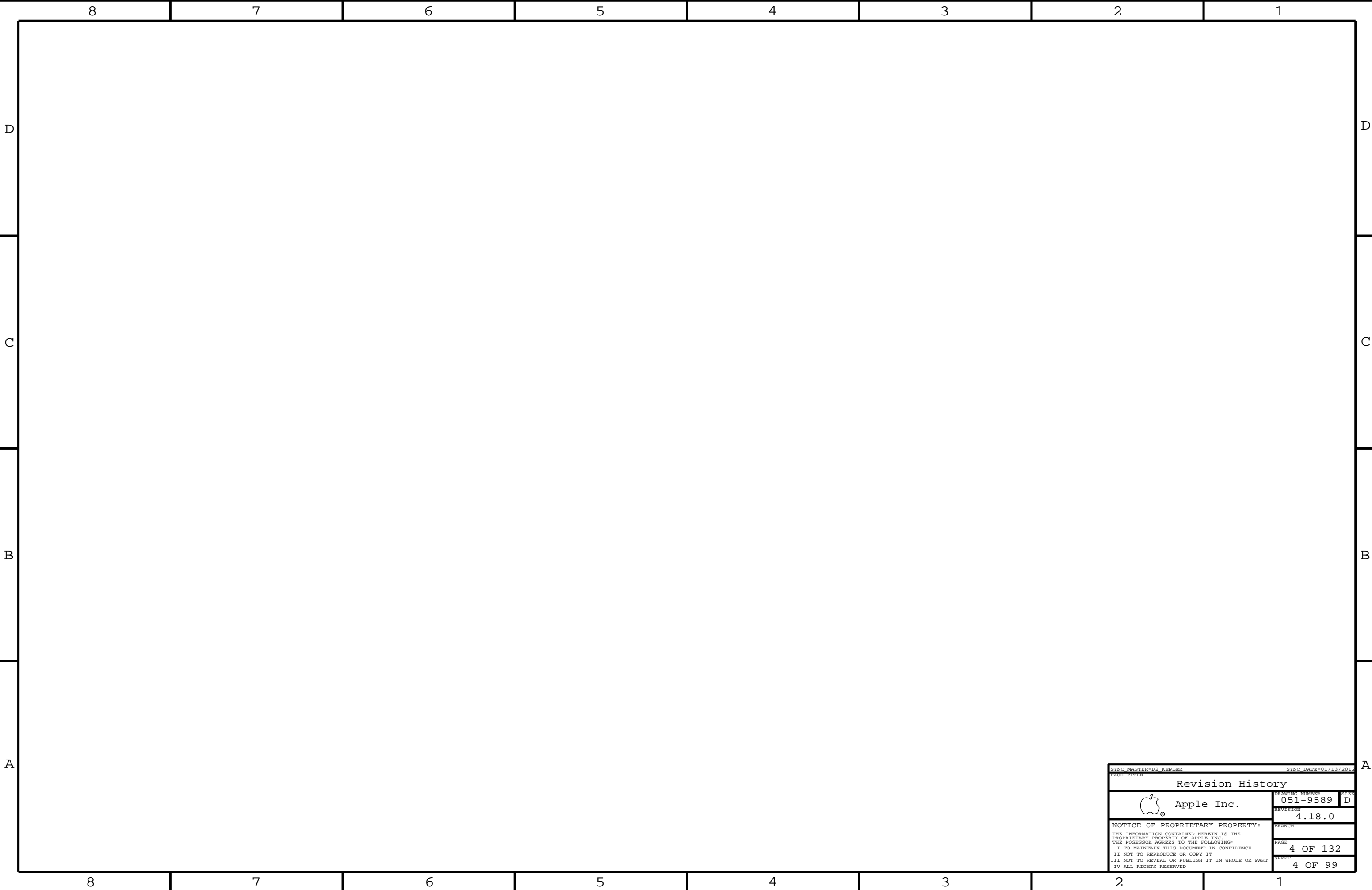
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PAGE
2 OF 132

SHEET
2 OF 99

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Revision History

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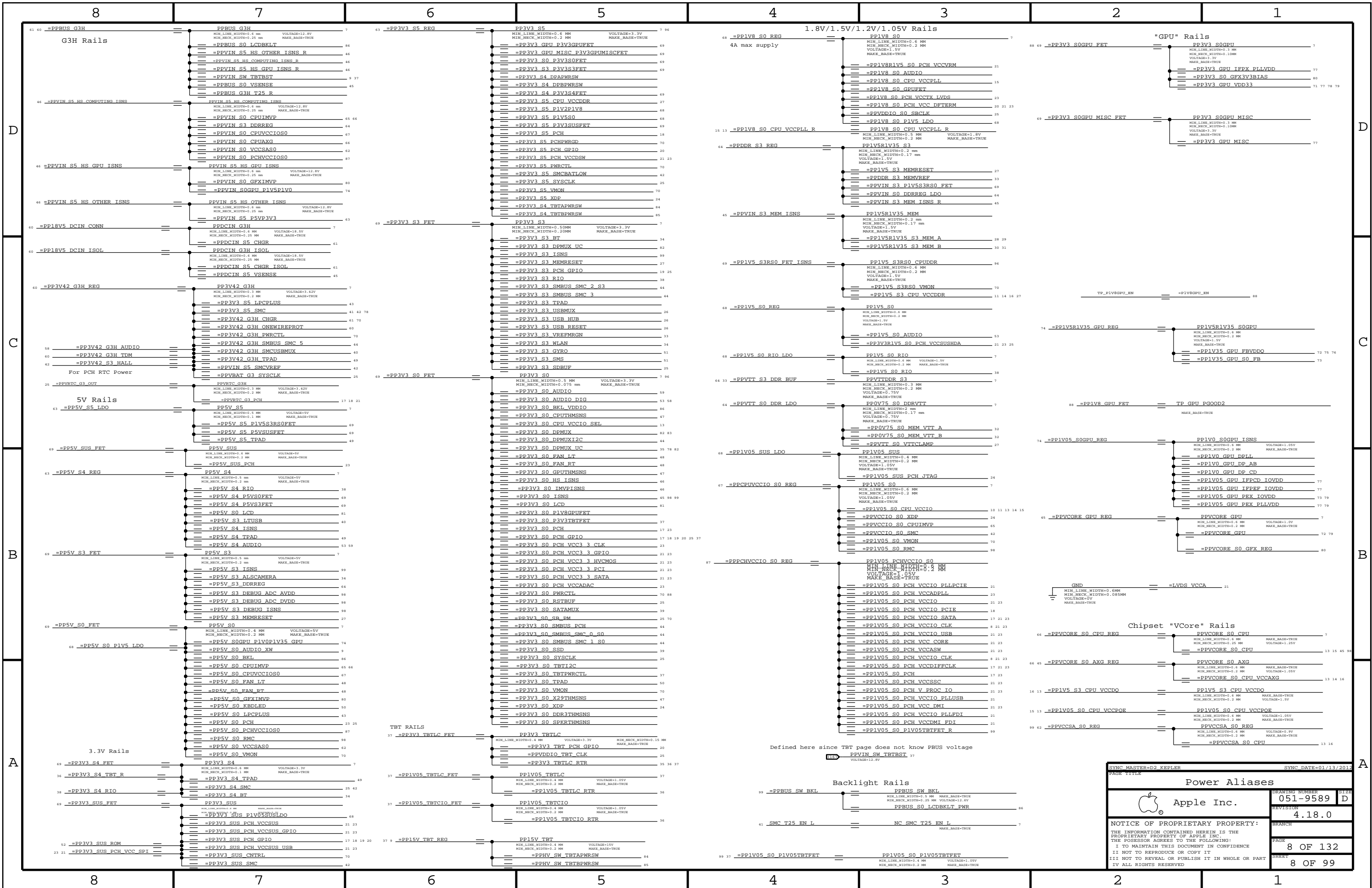
PAGE
4 OF 132

SHEET
4 OF 99

SIZE
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	BOM Variants (continued on CSA 6)																																																																																																																																																																				
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>085-3726</td><td>D2,MLB,KEPLER,DEV</td><td>D2_DEVEL:ENG</td></tr><tr><td>085-4776</td><td>D2,MLB,KEPLER,FSB DEV</td><td>D2_DEVEL:FSB</td></tr><tr><td>607-9546</td><td>D2,MLB,KEPLER_2PHASE,COMMON</td><td>D2_COMMON,POSCAP_MYLAR_PAIR</td></tr><tr><td>685-0016</td><td>PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2</td><td>PBUS_CAP:KEMET</td></tr><tr><td>685-0017</td><td>PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2</td><td>PBUS_CAP:SANYO</td></tr><tr><td>639-3378</td><td>PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3379</td><td>PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3380</td><td>PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3381</td><td>PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3384</td><td>PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3385</td><td>PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3386</td><td>PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3387</td><td>PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-2821</td><td>PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-2825</td><td>PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-2817</td><td>PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-2815</td><td>PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-2979</td><td>PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-2980</td><td>PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-2981</td><td>PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-2982</td><td>PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3618</td><td>PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3619</td><td>PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3561</td><td>PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3620</td><td>PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3627</td><td>PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3562</td><td>PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3628</td><td>PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3629</td><td>PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG	085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB	607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR	685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET	685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO	639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600	639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600	639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600	639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600	639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																			
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639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
	BOM Groups																																																																																																																																																																				
	<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>D2_COMMON</td><td>ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB</td></tr><tr><td>D2_COMMON1</td><td>CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRHT:PRQ,TBTRHT:Y,TBTHV:P15V,HUB_2KONKEM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V50:LDO</td></tr><tr><td>D2_COMMON2</td><td>EDP:YES,MIKEY,POPCOVOCIO:IVB,PGDOR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BLSANDEMIX,CAPS:INT,STPWR:S4,XDP_XDP_CPU:BDW,GPU:2P,TPAD_5V:LDO,S5</td></tr><tr><td>D2_PVB</td><td>VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:W</td></tr><tr><td>D2_PROGPARTS</td><td>SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG</td></tr><tr><td>D2_DEVEL:ENG</td><td>ALTERNATE,IVB_PPT_XDP,S0GOOD_IS1,SMC_DEBUG,DSRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV</td></tr><tr><td>D2_DEVEL:FSB</td><td>ALTERNATE,IVB_PPT_XDP</td></tr><tr><td>IVB_PPT_XDP</td><td>XDP_CONN,XDP_PCH</td></tr></table>								BOM GROUP	BOM OPTIONS	D2_COMMON	ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB	D2_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRHT:PRQ,TBTRHT:Y,TBTHV:P15V,HUB_2KONKEM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V50:LDO	D2_COMMON2	EDP:YES,MIKEY,POPCOVOCIO:IVB,PGDOR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BLSANDEMIX,CAPS:INT,STPWR:S4,XDP_XDP_CPU:BDW,GPU:2P,TPAD_5V:LDO,S5	D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:W	D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG	D2_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,S0GOOD_IS1,SMC_DEBUG,DSRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV	D2_DEVEL:FSB	ALTERNATE,IVB_PPT_XDP	IVB_PPT_XDP	XDP_CONN,XDP_PCH																																																																																																																																											
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D2_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRHT:PRQ,TBTRHT:Y,TBTHV:P15V,HUB_2KONKEM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V50:LDO																																																																																																																																																																				
D2_COMMON2	EDP:YES,MIKEY,POPCOVOCIO:IVB,PGDOR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BLSANDEMIX,CAPS:INT,STPWR:S4,XDP_XDP_CPU:BDW,GPU:2P,TPAD_5V:LDO,S5																																																																																																																																																																				
D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:W																																																																																																																																																																				
D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG																																																																																																																																																																				
D2_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,S0GOOD_IS1,SMC_DEBUG,DSRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV																																																																																																																																																																				
D2_DEVEL:FSB	ALTERNATE,IVB_PPT_XDP																																																																																																																																																																				
IVB_PPT_XDP	XDP_CONN,XDP_PCH																																																																																																																																																																				
	Module Parts																																																																																																																																																																				
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>33784266</td><td>1</td><td>10V,8 800M,PAQ,81,2,3,40A,4+2,1,2,6M,MOA</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_SGE</td></tr><tr><td>33784267</td><td>1</td><td>10V,8 800M,PAQ,81,2,4,40A,4+2,1,25,6M,MOA</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_SGHZ</td></tr><tr><td>33784268</td><td>1</td><td>10V,8 800M,PAQ,81,2,7,40A,4+2,1,25,6M,MOA</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_SGHZ</td></tr><tr><td>33784269</td><td>1</td><td>PANVIEW,PO30RT,C1,EL29C,PAQ,MOB30M77</td><td>U1800</td><td>CRITICAL</td><td></td></tr><tr><td>33784256</td><td>1</td><td>10,0PU,MY,08107-075-40-A3</td><td>U8000</td><td>CRITICAL</td><td></td></tr><tr><td>33881113</td><td>1</td><td>10,70V,10-40,80,PAQ,C10,228 12012 90-10P</td><td>U3600</td><td>CRITICAL</td><td>TBTROM:FSB</td></tr><tr><td>33380622</td><td>32</td><td>10,800M,2083-1600,250009,78P90A,8V1X,C-DIE,180M</td><td></td><td>CRITICAL</td><td>2G_HYNIX_1600</td></tr><tr><td>33380623</td><td>32</td><td>10,800M,2083-1600,250009,78P90A,8V1X</td><td></td><td>CRITICAL</td><td>2G_SAMSUNG_1600</td></tr><tr><td>33380628</td><td>32</td><td>10,800M,2083-1600,250009,78P90A,8-CIE,ELPIDA</td><td></td><td>CRITICAL</td><td>2G_ELPIDA_1600</td></tr><tr><td>33380625</td><td>32</td><td>10,800M,2083-1600,512009,78P90A,8V1X</td><td></td><td>CRITICAL</td><td>4G_HYNIX_1600</td></tr><tr><td>33380624</td><td>32</td><td>10,800M,2083-1600,512009,78P90A,C-DIE,SANCI80</td><td></td><td>CRITICAL</td><td>4G_SAMSUNG_1600</td></tr><tr><td>33380629</td><td>32</td><td>10,800M,2083-1600,512009,78P90A,8-CIE,ELPIDA</td><td></td><td>CRITICAL</td><td>4G_ELPIDA_1600</td></tr><tr><td>33380630</td><td>4</td><td>10,800M,20205,64Mx12,A-DIE,HYNIX</td><td>U8400,U8450,U8500,U8550</td><td>CRITICAL</td><td>FB_2G_HYNIX_A_DIE</td></tr><tr><td>33380631</td><td>4</td><td>10,800M,20205,64Mx12,B-DIE,SANCI80</td><td>U8400,U8450,U8500,U8550</td><td>CRITICAL</td><td>FB_2G_SAMSUNG</td></tr><tr><td>12850264</td><td>30</td><td>CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E</td><td></td><td>CRITICAL</td><td>PBUS_CAP:SANYO</td></tr><tr><td>12850257</td><td>30</td><td>CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF</td><td></td><td>CRITICAL</td><td>PBUS_CAP:KEMET</td></tr><tr><td>725-1614</td><td>1</td><td>INSULATOR,SHORT,REAR,MLB,D2</td><td>REAR_INSULATOR</td><td>CRITICAL</td><td>PBUS_CAP:SANYO</td></tr><tr><td>725-1648</td><td>1</td><td>INSULATOR,TALL,REAR,MLB,D2</td><td>REAR_INSULATOR</td><td>CRITICAL</td><td>PBUS_CAP:KEMET</td></tr><tr><td>725-1568</td><td>1</td><td>INSULATOR,CPU,D2</td><td>CPU_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>725-1569</td><td>1</td><td>INSULATOR,GPU,D2</td><td>GPU_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>725-1621</td><td>1</td><td>INSULATOR,PCH,D2</td><td>PCH_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>806-2897</td><td>2</td><td>CAN_COVER,2,J5</td><td>CAN_COVER1,CAN_COVER2</td><td>CRITICAL</td><td></td></tr><tr><td>825-7697</td><td>1</td><td>TEXT,LABEL,MLB,D2</td><td>TEXT_LABEL</td><td>CRITICAL</td><td></td></tr><tr><td>946-3819</td><td>1</td><td>D2 MLB DYNAX ADHESIVE SRE-CURE 29993-SC</td><td>EDGE_BOND</td><td>CRITICAL</td><td></td></tr><tr><td>825-7841</td><td>1</td><td>LBL,PART CONFIG,BOARDS,D2</td><td>CONFIG_LABEL</td><td>CRITICAL</td><td></td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	33784266	1	10V,8 800M,PAQ,81,2,3,40A,4+2,1,2,6M,MOA	U1000	CRITICAL	CPU_IVV:2_SGE	33784267	1	10V,8 800M,PAQ,81,2,4,40A,4+2,1,25,6M,MOA	U1000	CRITICAL	CPU_IVV:2_SGHZ	33784268	1	10V,8 800M,PAQ,81,2,7,40A,4+2,1,25,6M,MOA	U1000	CRITICAL	CPU_IVV:2_SGHZ	33784269	1	PANVIEW,PO30RT,C1,EL29C,PAQ,MOB30M77	U1800	CRITICAL		33784256	1	10,0PU,MY,08107-075-40-A3	U8000	CRITICAL		33881113	1	10,70V,10-40,80,PAQ,C10,228 12012 90-10P	U3600	CRITICAL	TBTROM:FSB	33380622	32	10,800M,2083-1600,250009,78P90A,8V1X,C-DIE,180M		CRITICAL	2G_HYNIX_1600	33380623	32	10,800M,2083-1600,250009,78P90A,8V1X		CRITICAL	2G_SAMSUNG_1600	33380628	32	10,800M,2083-1600,250009,78P90A,8-CIE,ELPIDA		CRITICAL	2G_ELPIDA_1600	33380625	32	10,800M,2083-1600,512009,78P90A,8V1X		CRITICAL	4G_HYNIX_1600	33380624	32	10,800M,2083-1600,512009,78P90A,C-DIE,SANCI80		CRITICAL	4G_SAMSUNG_1600	33380629	32	10,800M,2083-1600,512009,78P90A,8-CIE,ELPIDA		CRITICAL	4G_ELPIDA_1600	33380630	4	10,800M,20205,64Mx12,A-DIE,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE	33380631	4	10,800M,20205,64Mx12,B-DIE,SANCI80	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG	12850264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO	12850257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET	725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO	725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET	725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL		725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL		725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL		806-2897	2	CAN_COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL		825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL		946-3819	1	D2 MLB DYNAX ADHESIVE SRE-CURE 29993-SC	EDGE_BOND	CRITICAL		825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL		
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33380623	32	10,800M,2083-1600,250009,78P90A,8V1X		CRITICAL	2G_SAMSUNG_1600																																																																																																																																																																
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33380624	32	10,800M,2083-1600,512009,78P90A,C-DIE,SANCI80		CRITICAL	4G_SAMSUNG_1600																																																																																																																																																																
33380629	32	10,800M,2083-1600,512009,78P90A,8-CIE,ELPIDA		CRITICAL	4G_ELPIDA_1600																																																																																																																																																																
33380630	4	10,800M,20205,64Mx12,A-DIE,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE																																																																																																																																																																
33380631	4	10,800M,20205,64Mx12,B-DIE,SANCI80	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG																																																																																																																																																																
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725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO																																																																																																																																																																
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET																																																																																																																																																																
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL																																																																																																																																																																	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL																																																																																																																																																																	
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BOM Variants (continued from CSA 5)			Bar Code Labels / EEEE #'s (continued from CSA 5)					
BOM NUMBER	BOM NAME	BOM OPTIONS	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
639-3382	PCBA, 2. 3G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DY41	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
639-3383	PCBA, 2. 3G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DY42	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
639-3445	PCBA, 2. 3G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DYJ5	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
639-3446	PCBA, 2. 3G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DYJ6	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
639-2818	PCBA, 2. 6G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRF0	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
639-2820	PCBA, 2. 6G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDP	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
639-2823	PCBA, 2. 6G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRDT	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
639-2819	PCBA, 2. 6G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDQ	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
639-3632	PCBA, 2. 7G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, F0JD	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
639-3633	PCBA, 2. 7G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, F0J3	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
639-3630	PCBA, 2. 7G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, F0J4	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
639-3631	PCBA, 2. 7G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, F0JC	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC
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SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

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Apple Inc.

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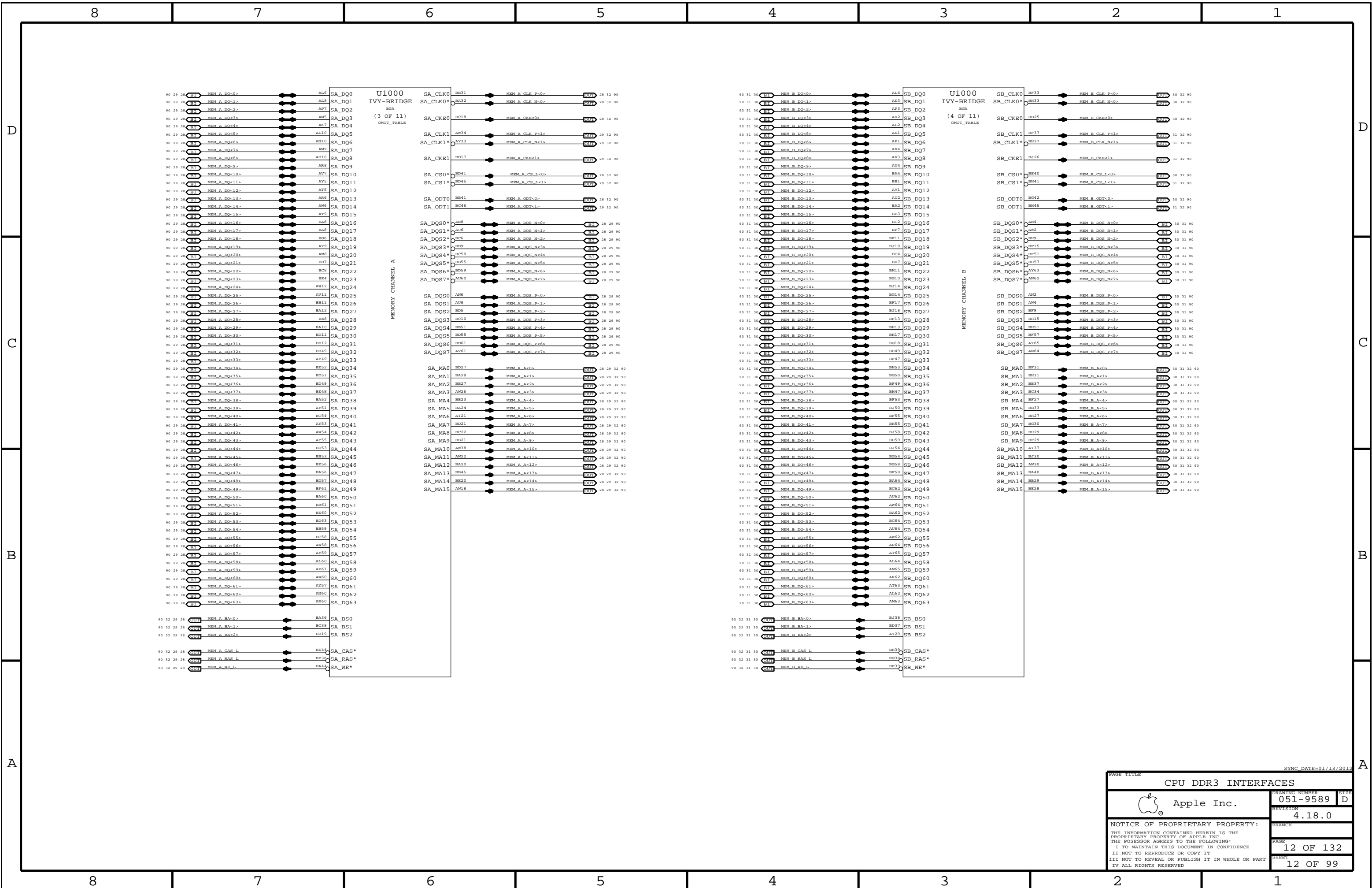
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PAGE
8 OF 132

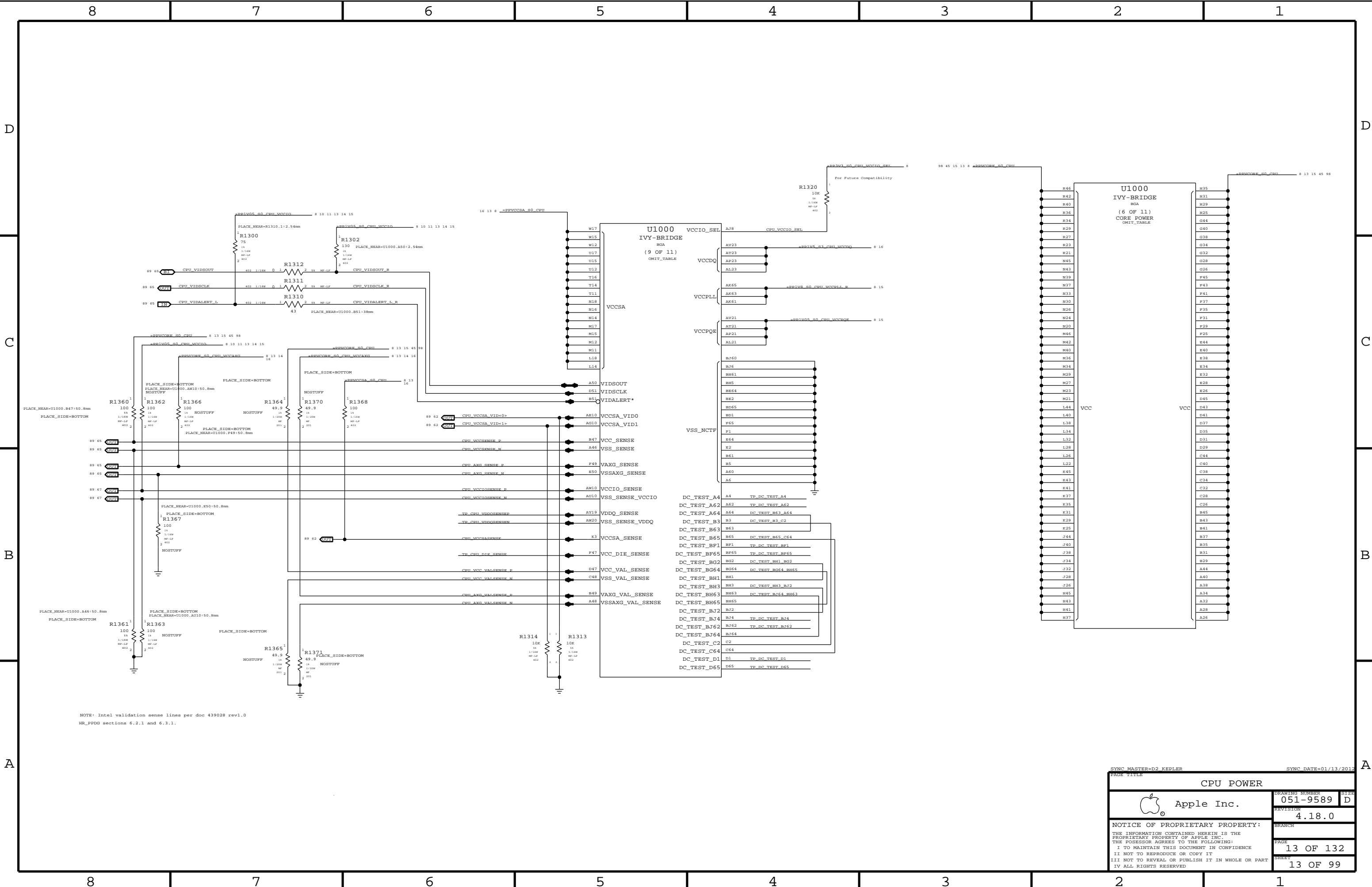
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8 OF 99







PAGE TITLE		CPU DDR3 INTERFACES	
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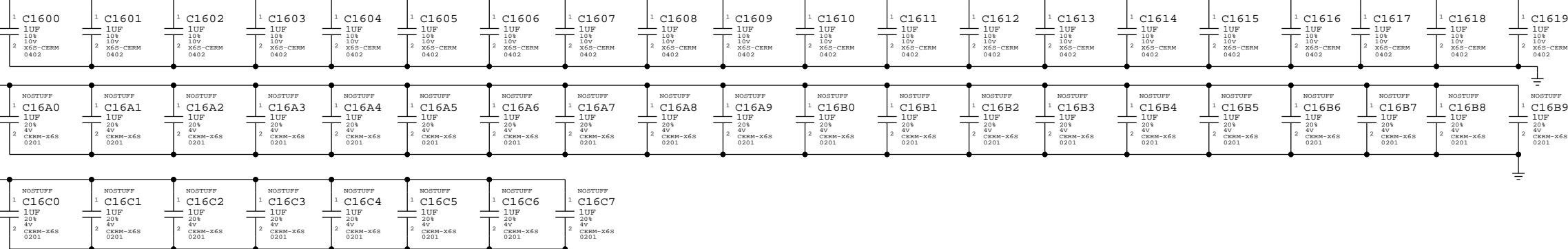
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

PAGE TITLE		PAGE NUMBER	
CPU POWER		4.18.0	
Apple Inc.		13 OF 132	
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Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm, 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

Place on bottom side of U1000



1 C1620 10UF 20% 4V X68 0402

1 C1621 10UF 20% 4V X68 0402

1 C1622 10UF 20% 4V X68 0402

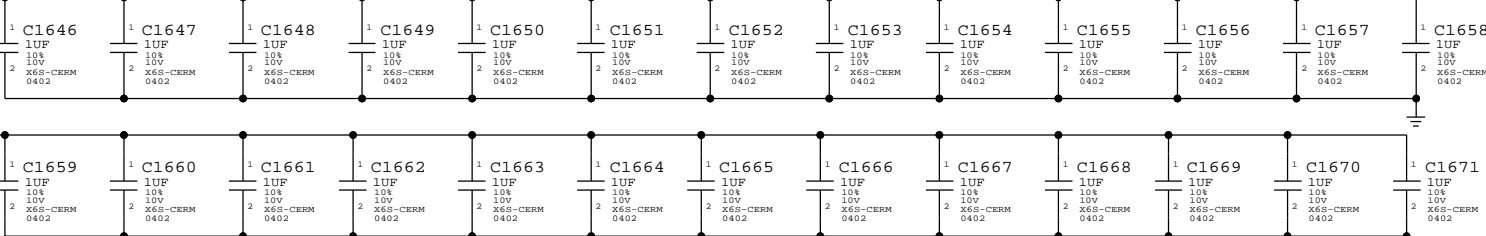
1 C1623 10UF 20% 4V X68 0402

[illegible]

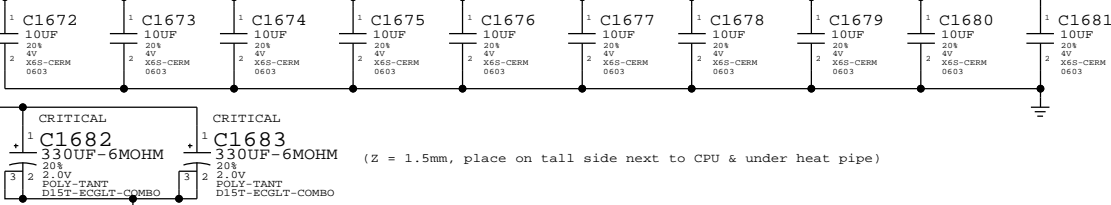
Figure 10 is a schematic diagram of the output filter, showing a series of eight identical filter stages connected in series. Each stage consists of a series inductor (L) and a shunt capacitor (C). The capacitors are labeled CRITICAL C1640 through C1689, with values of 270UF and 20% tolerance. The inductors are labeled TANT CASE-B2-SM with values of 2V. The diagram is a single-line schematic with ground connections at the input and output of each stage.

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

Place on bottom side of U1000



Place near U1000 on bottom side

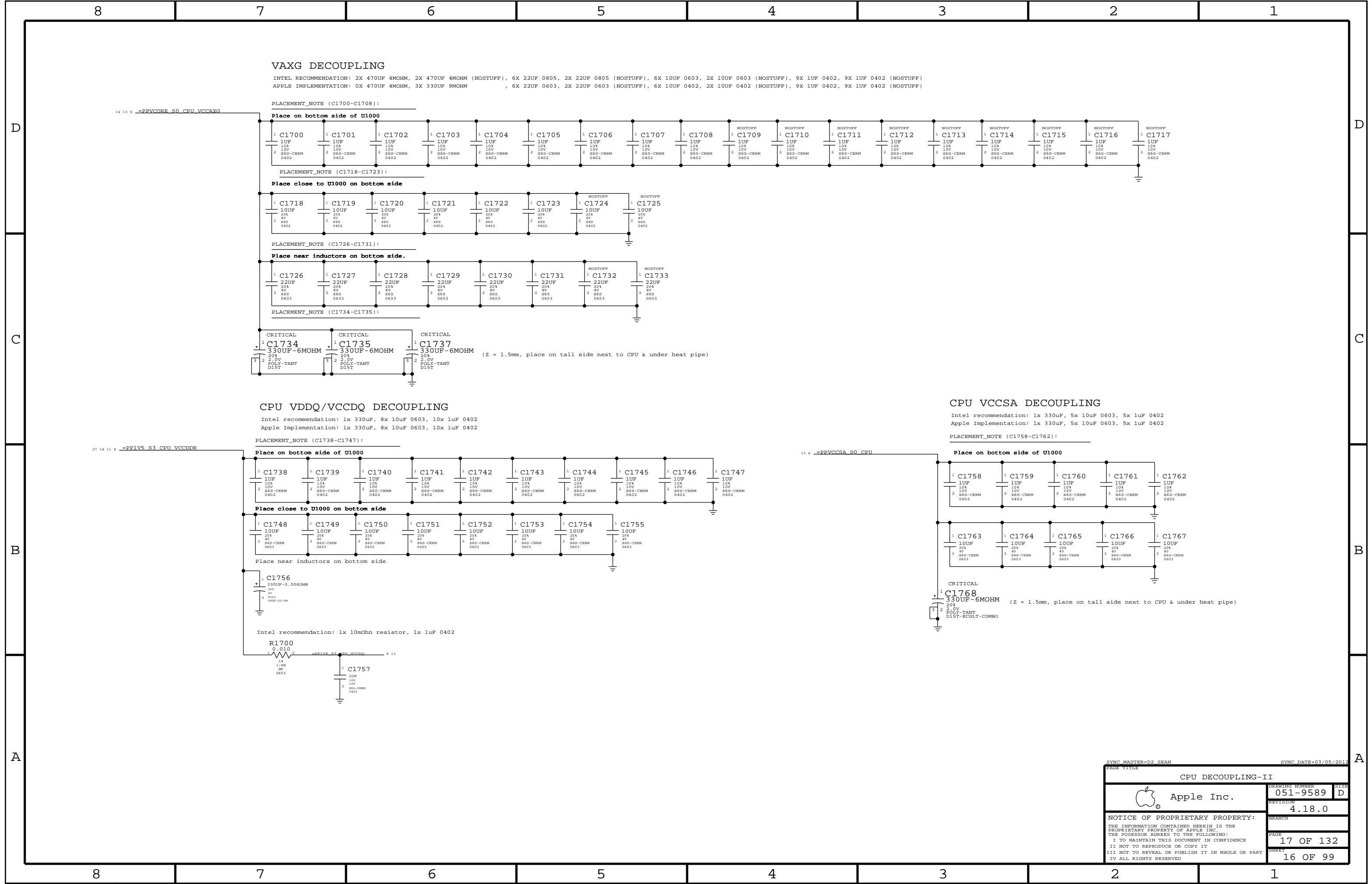


R1601
0.010
1%
1/4W
0603

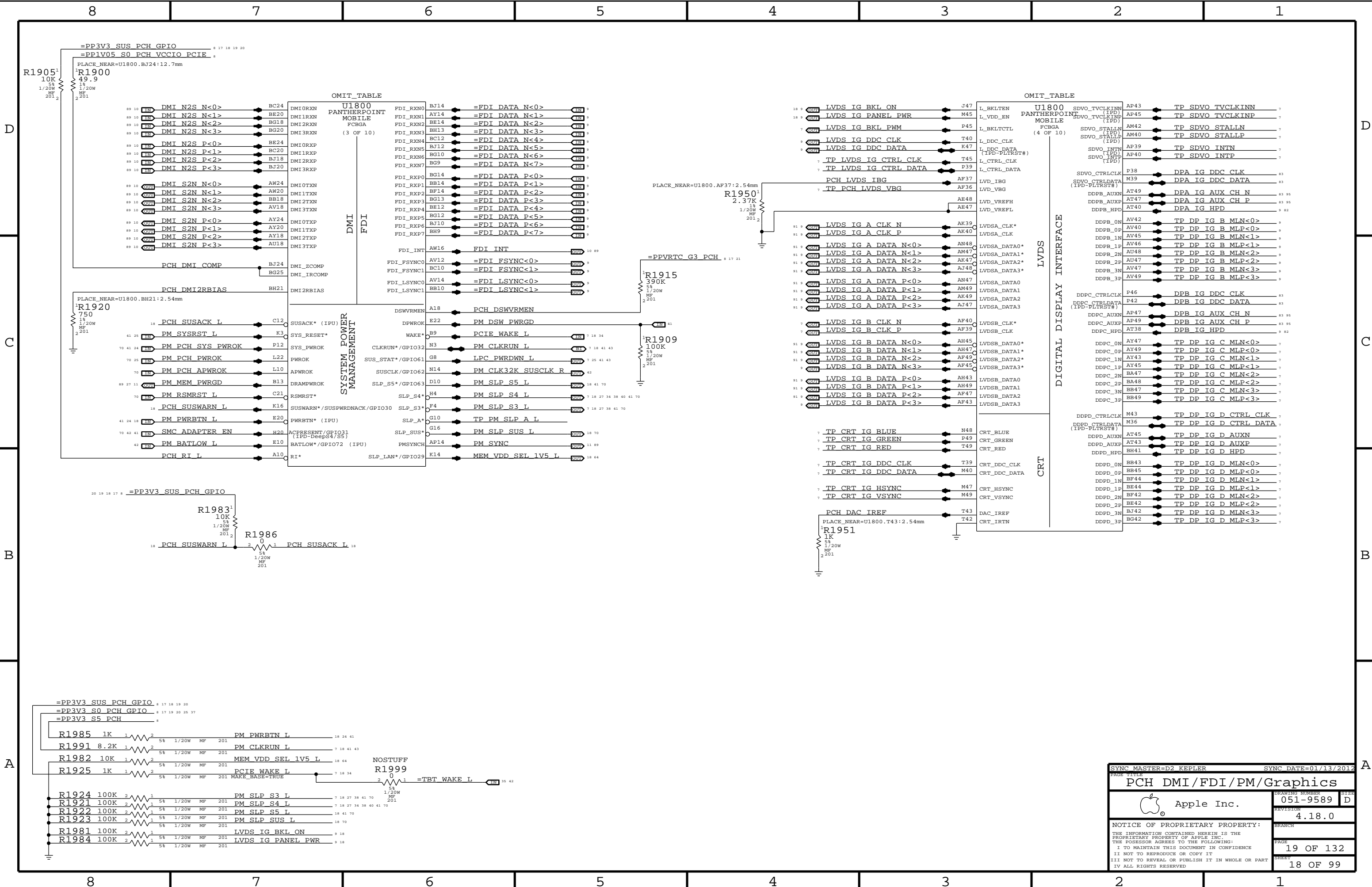
#PP1W05_S0 CPU_VCCP0E

C1684
1uF
10%
10V
X50-CERM
0402

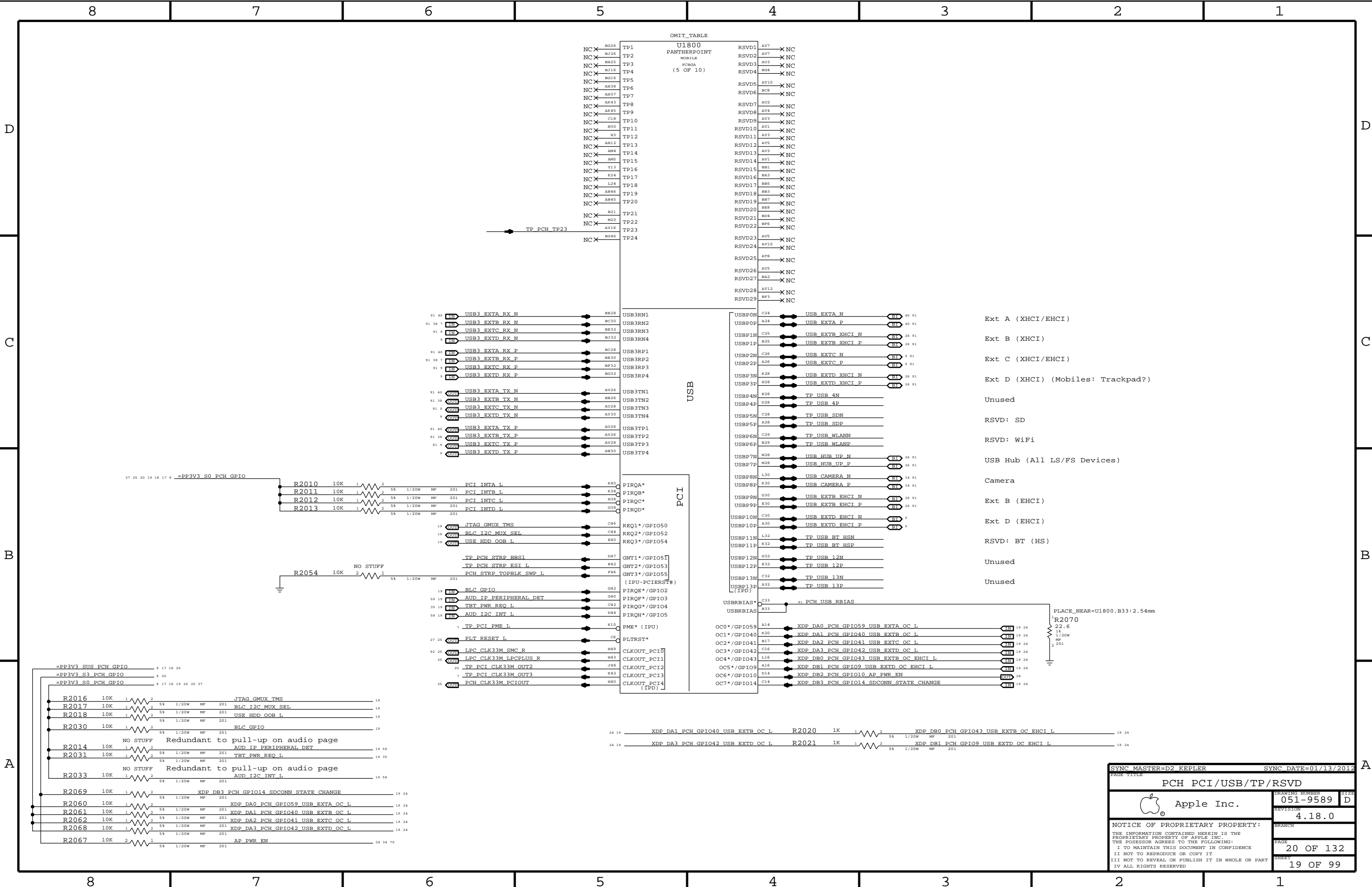
[illegible]







PAGE TITLE		PAGE NUMBER	
PCH DMI/FDI/PM/Graphics		051-9589	
Apple Inc.		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		19 OF 132	
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DRAWING NUMBER

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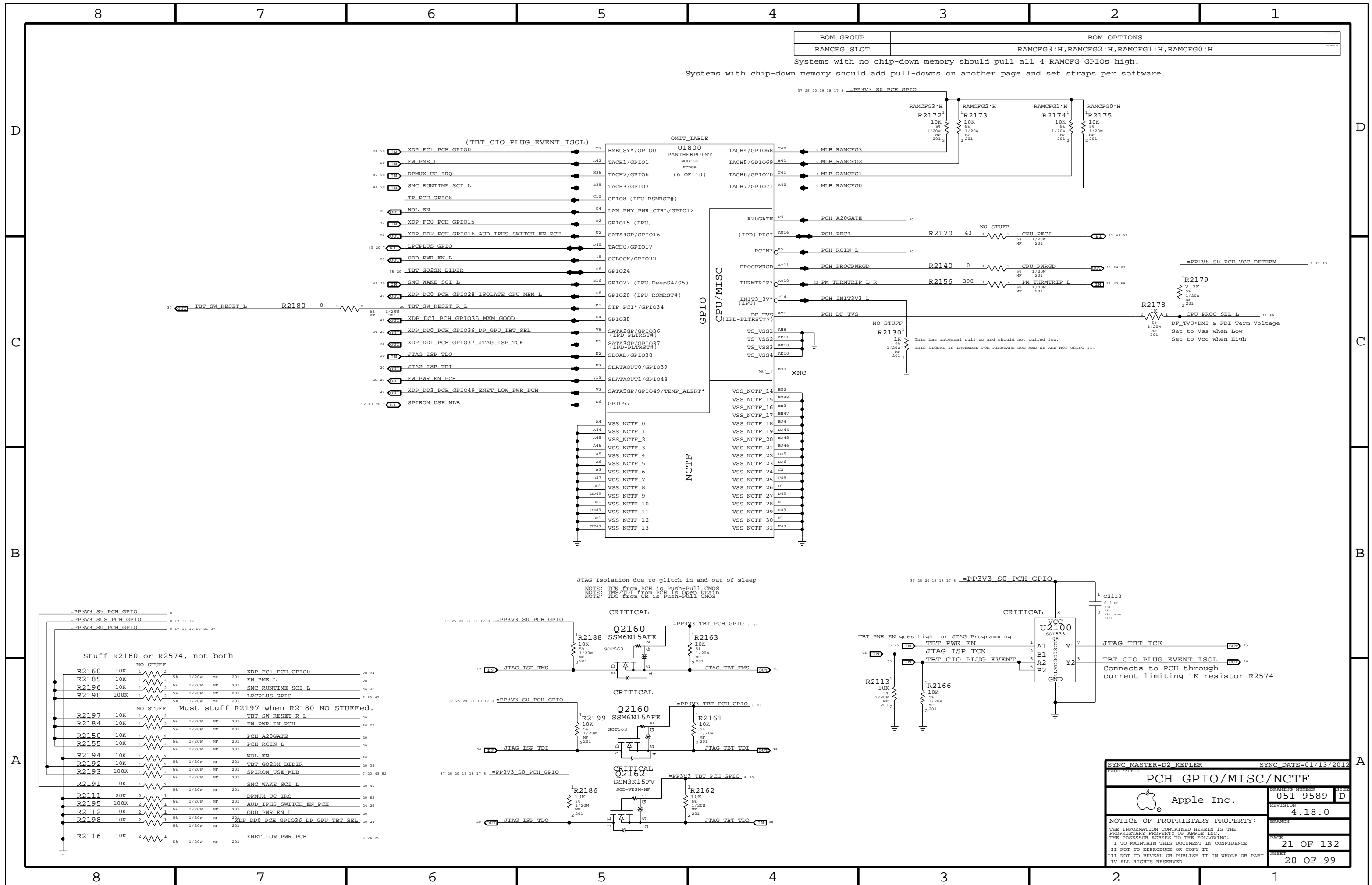
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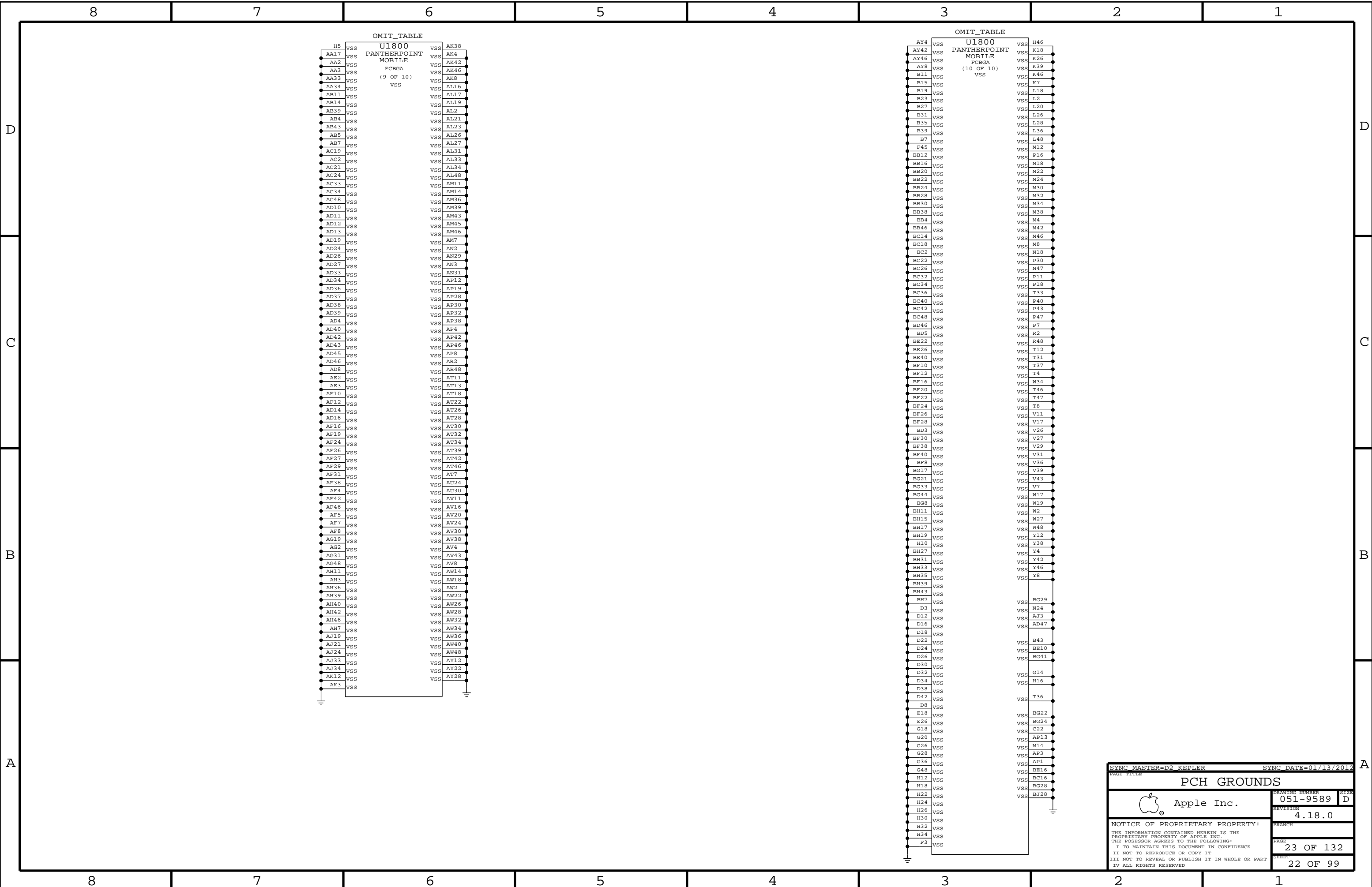
PAGE

20 OF 132

SHEET

19 OF 99






SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

PAGE TITLE

PCH GROUNDS

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DRAWING NUMBER
051-9589

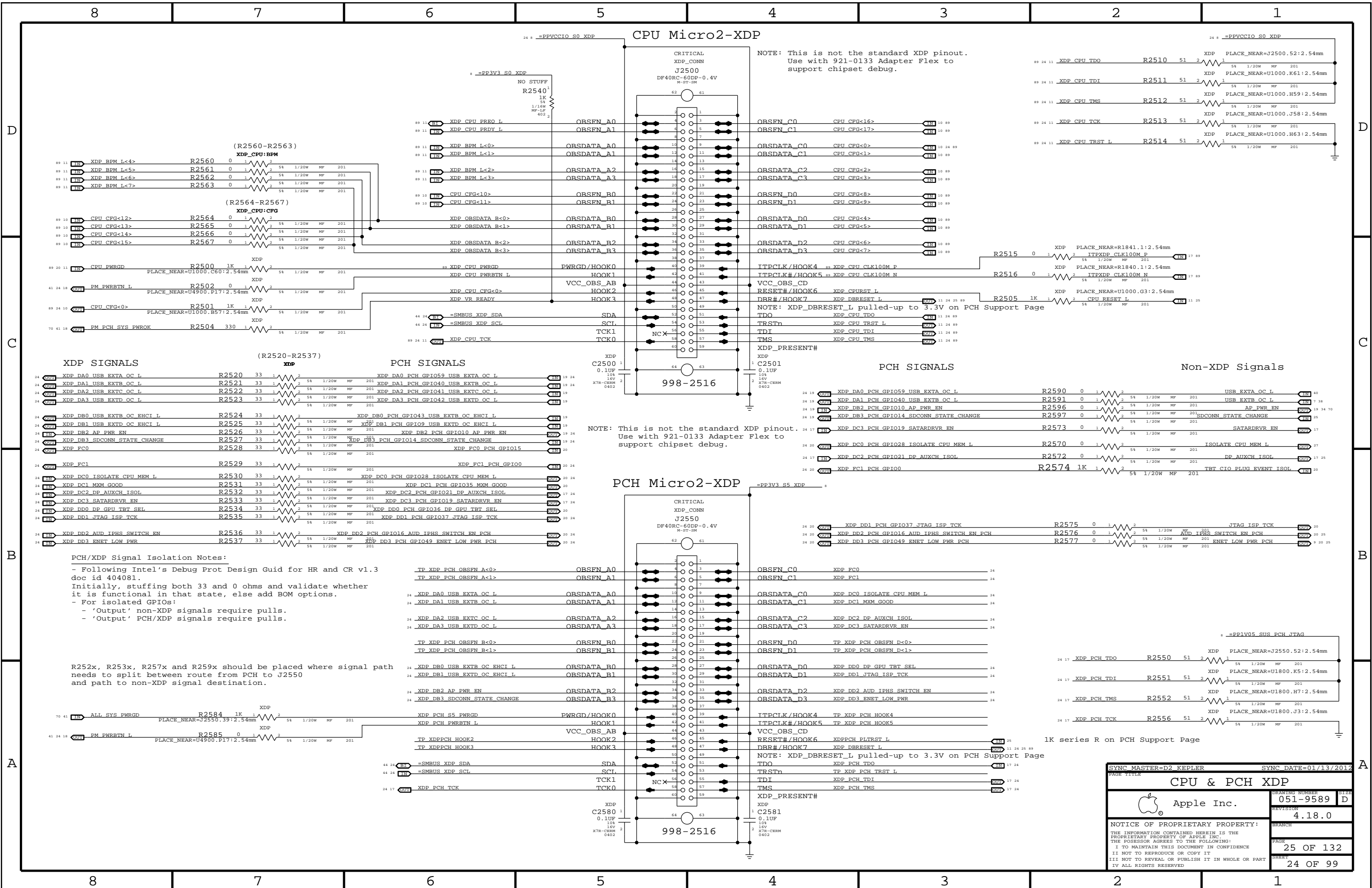
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BRANCH
PAGE
23 OF 132
SHEET
22 OF 99





D

D

C

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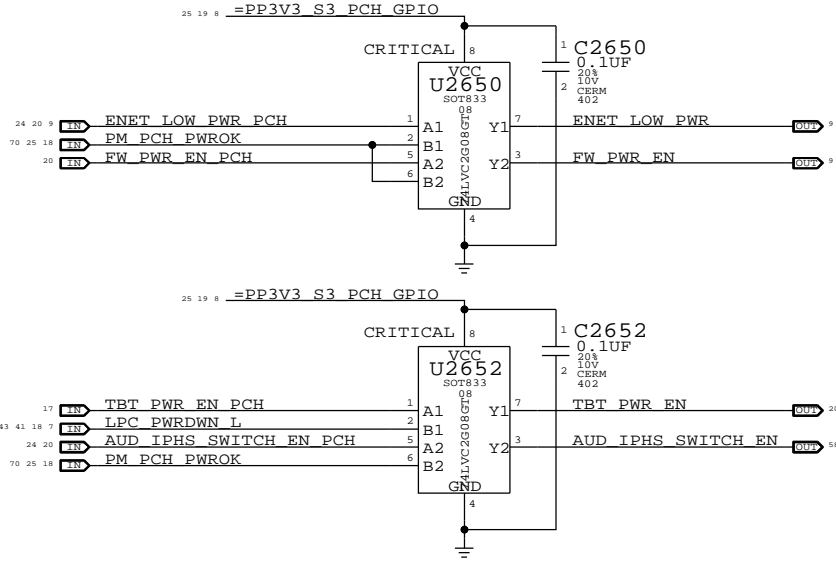
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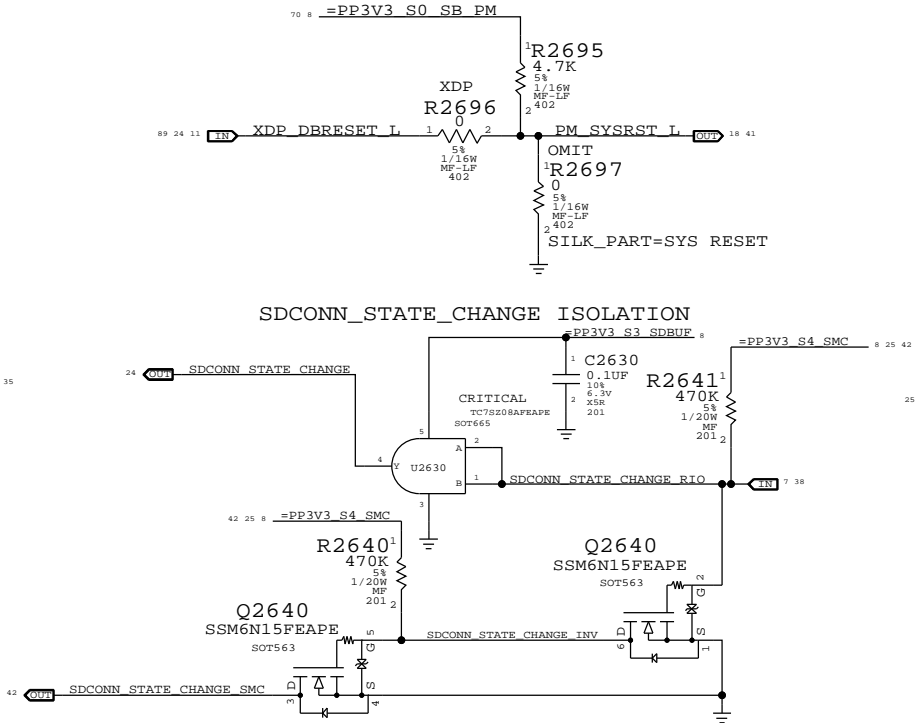
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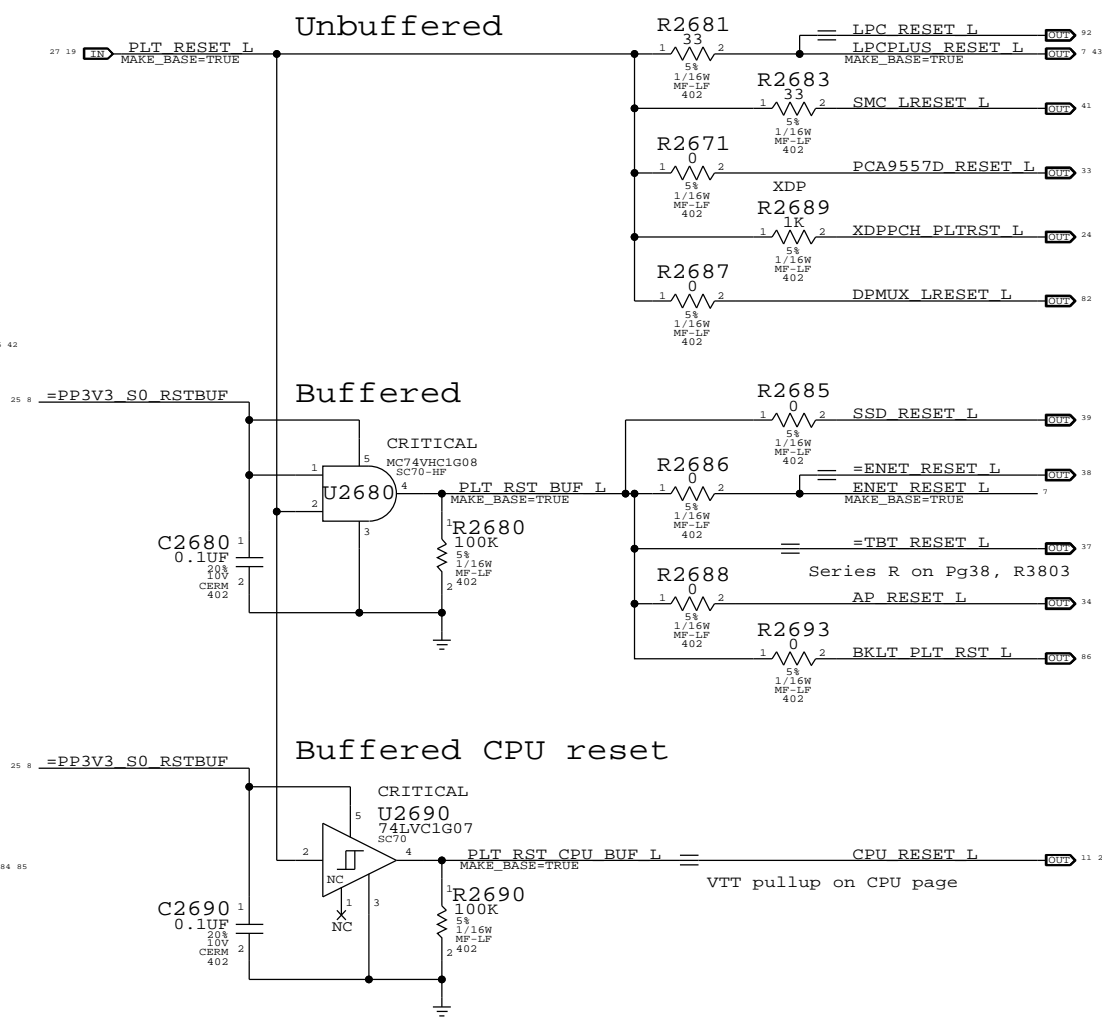
GPIO Glitch Prevention



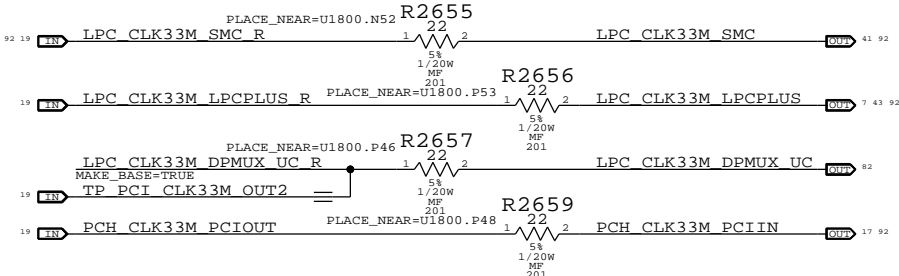
PCH Reset Button



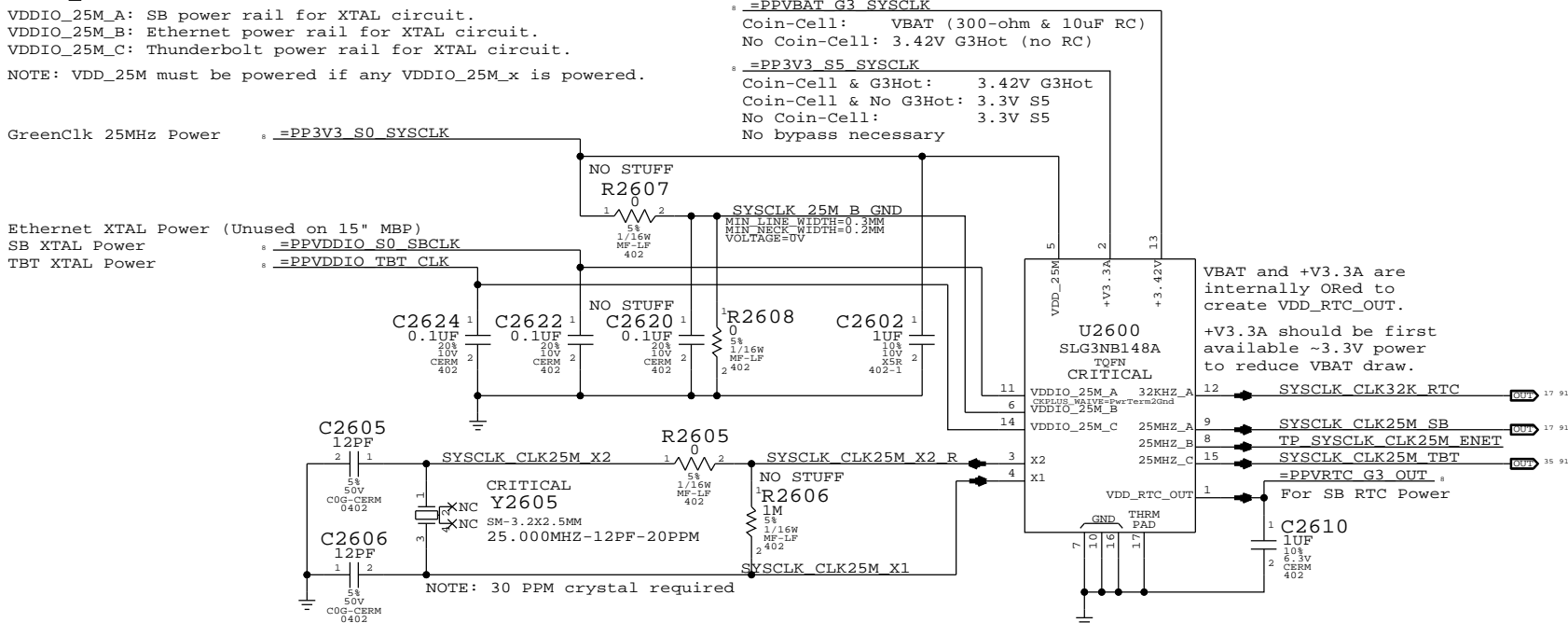
Platform Reset Connections



LPC 33MHz Clock Series Termination

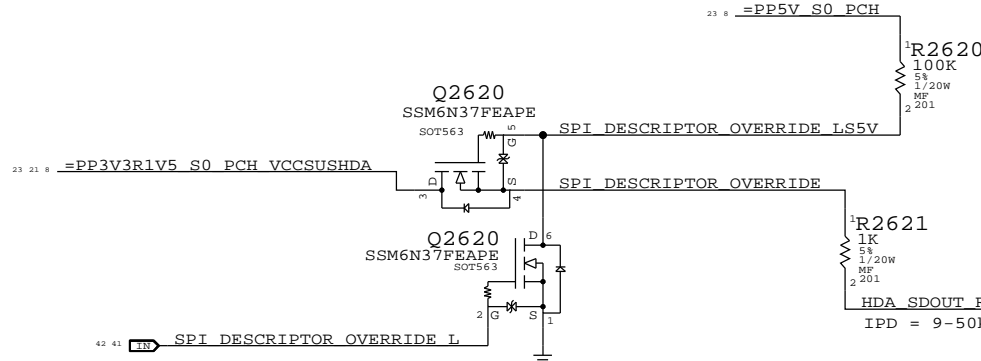



System RTC Power Source & 32kHz / 25MHz Clock Generator



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Chipset Support			
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		SHEET	D
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

```

NON_REM 1 :  NON_REM 0      STRAP PIN CFG
0           :  0             ALL PORTS ARE REMOVABLE
0           :  0             PORT 1 IS NON REMOVABLE
0           :  0             PORT 1&2 ARE NON REMOVABLE
1           :  1             PORT 1&2&3 ARE NON REMOVABLE

```

BOM TABLE

15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



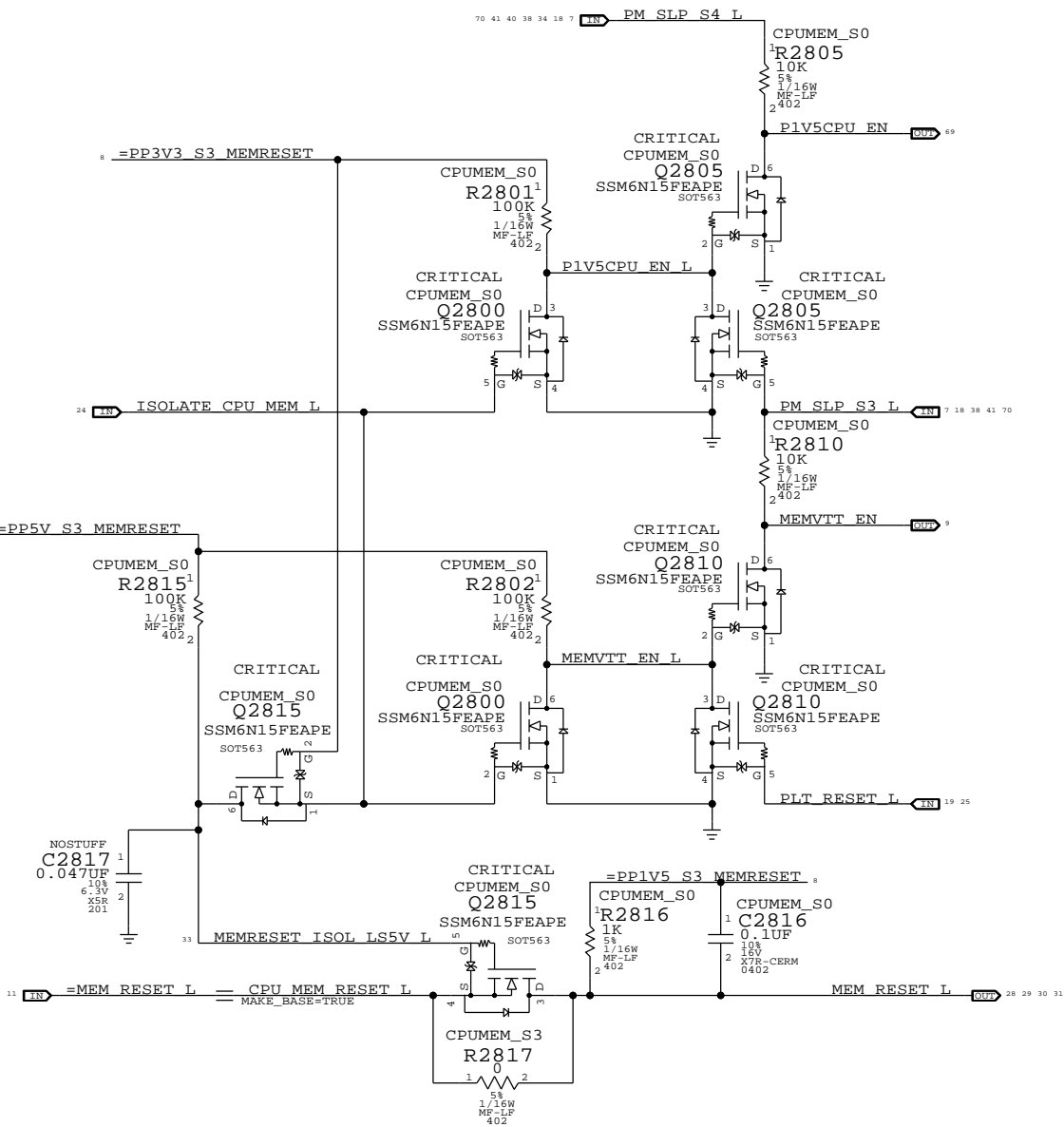
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

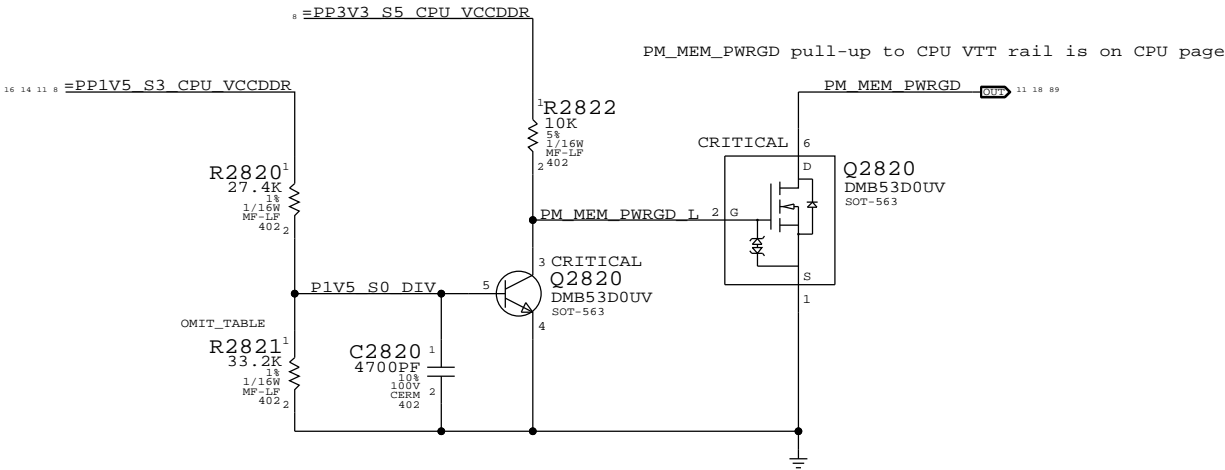
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



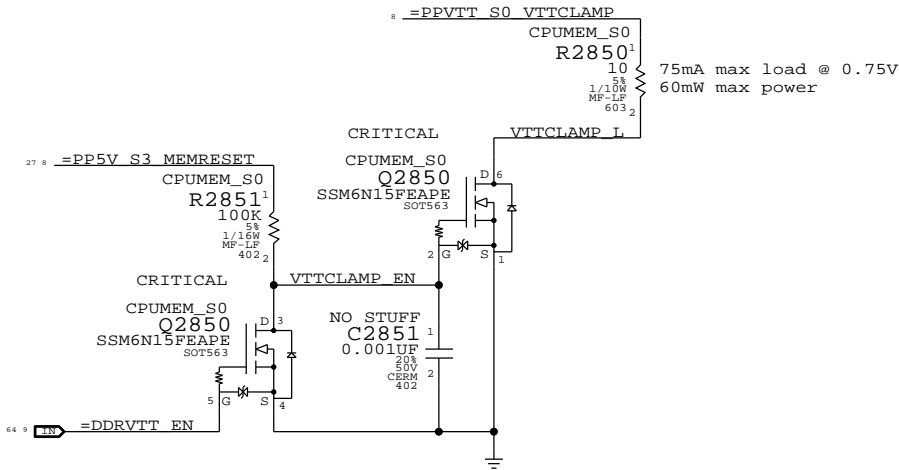
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES,MTL,P1M,1/16W,33,2K,1,0402,SMD,LF	R2821		PPDDR:1V5
114S0376	1	RES,MTL,P1M,1/16W,43,2K,1,0402,SMD,LF	R2821		PPDDR:1V35

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

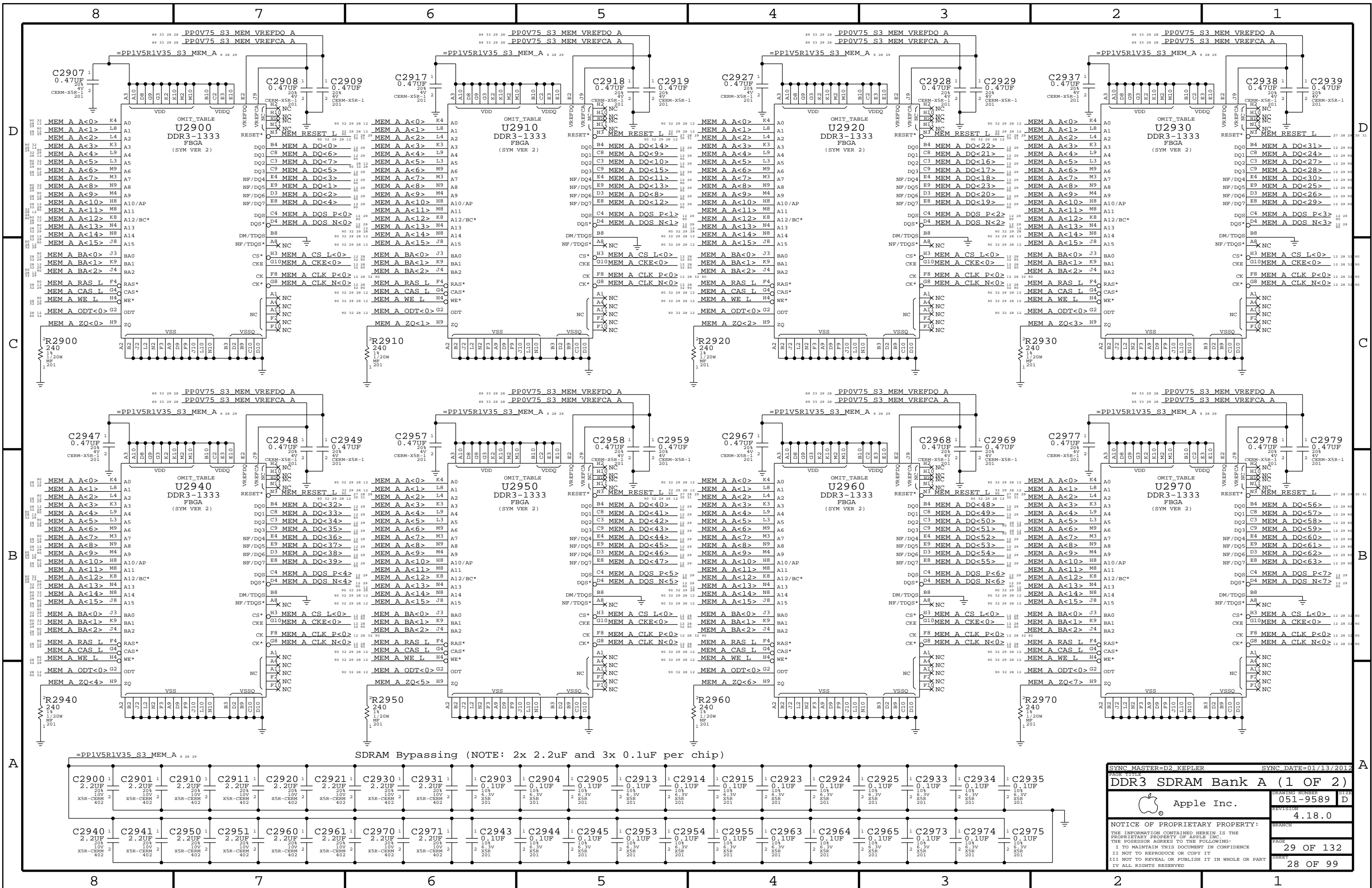


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

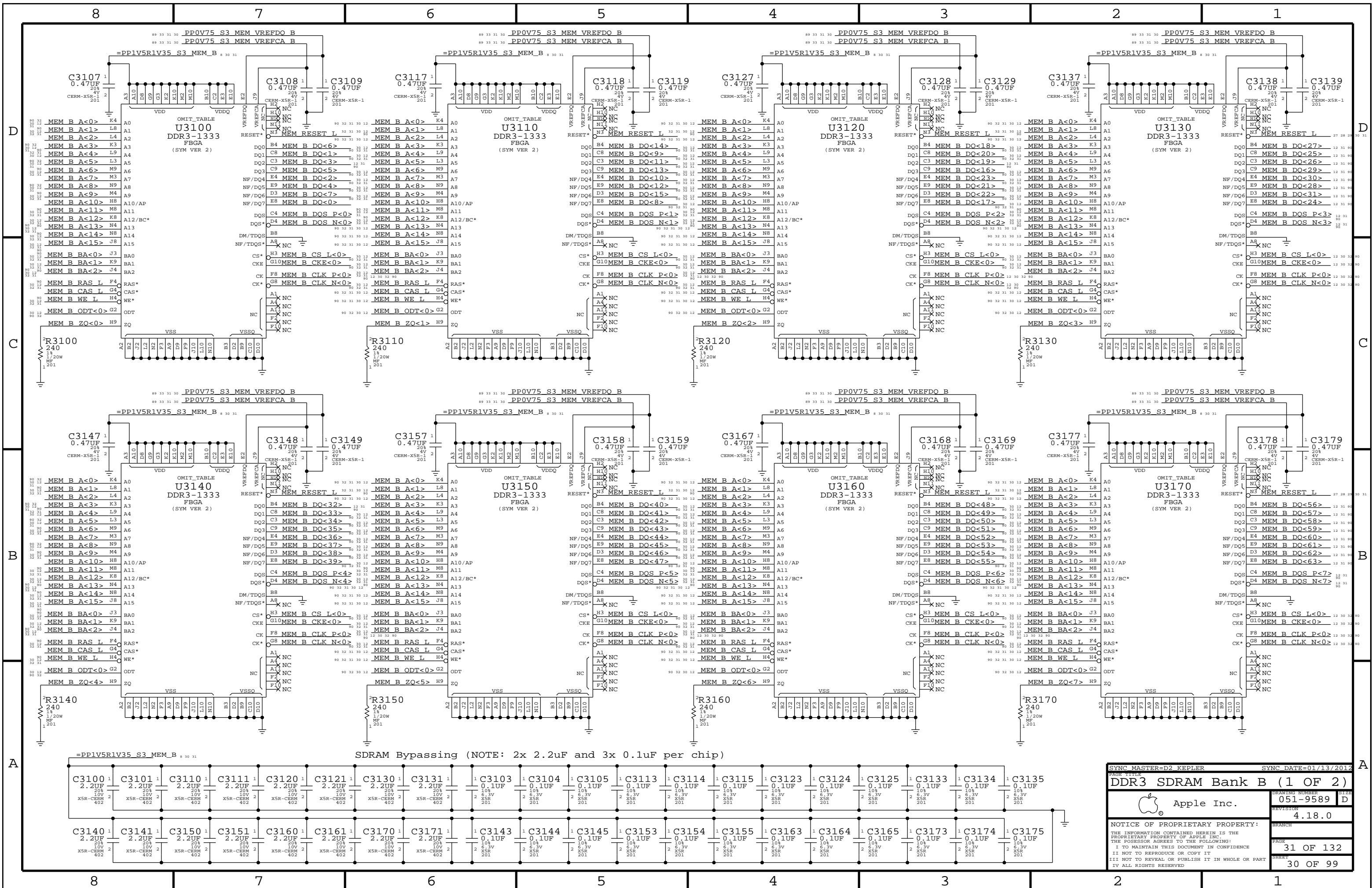
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE		CPU Memory S3 Support	
DRAWING NUMBER		051-9589	SIZE D
REVISION		4.18.0	BRANCH
PAGE		28 OF 132	SHEET
SHEET		27 OF 99	

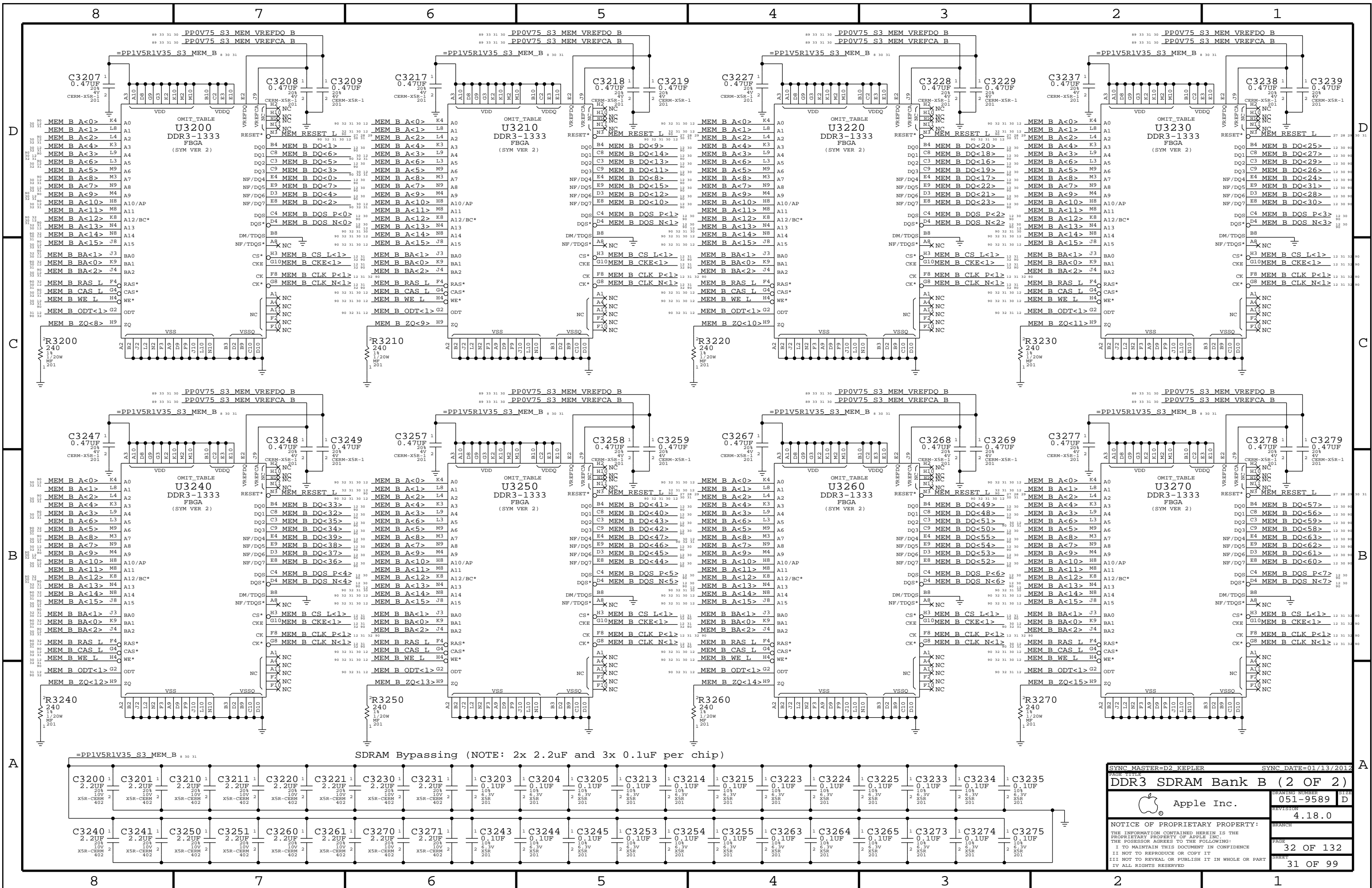



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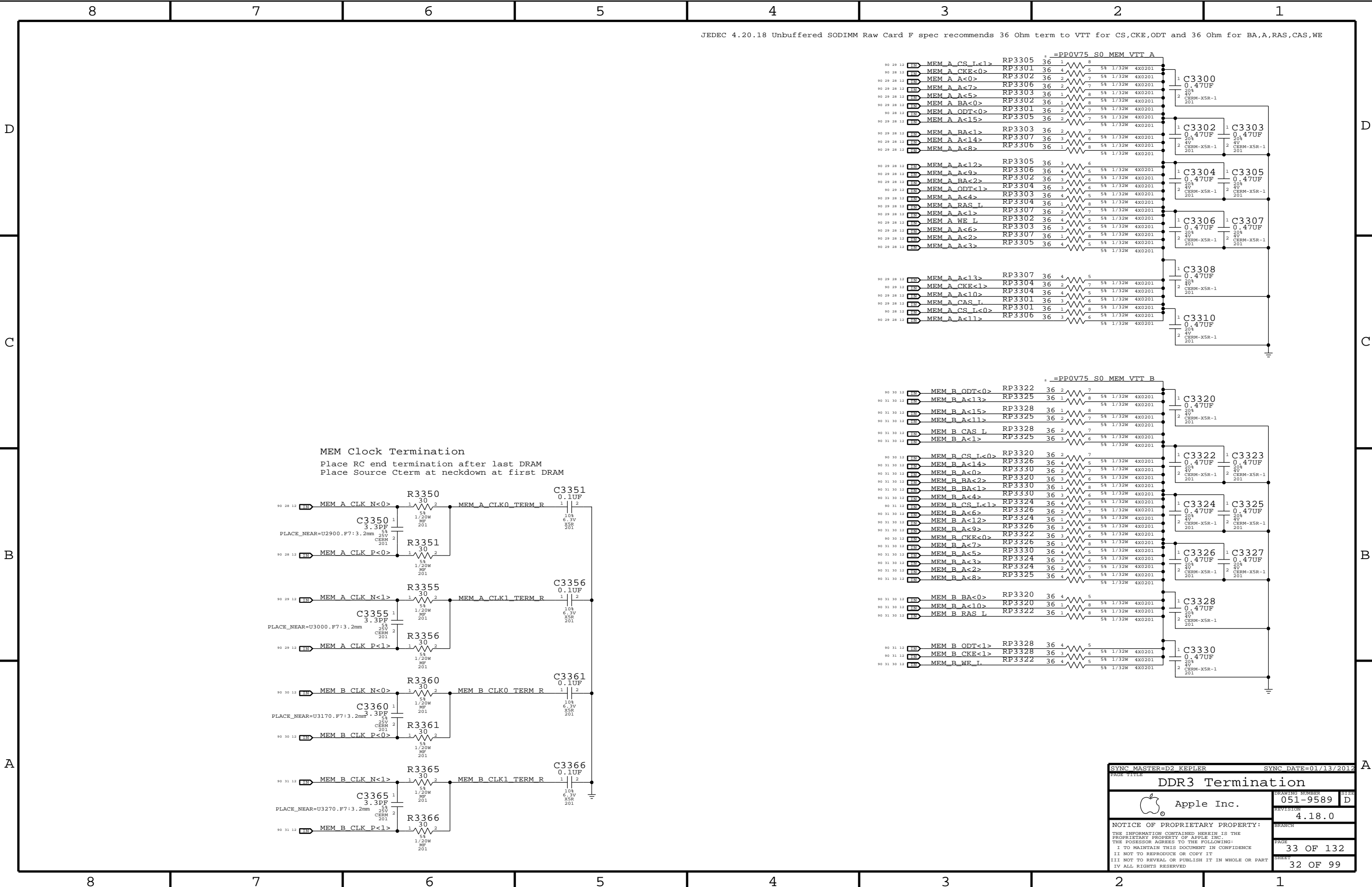




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BRANCH
PAGE
31 OF 132
SHEET
30 OF 99



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
DDR3 SDRAM Bank B		(2 OF 2)	
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		SHEET	31 OF 99




JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

MEM Clock Termination
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

DDR3 Termination

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PAGE
33 OF 132

SHEET
32 OF 99

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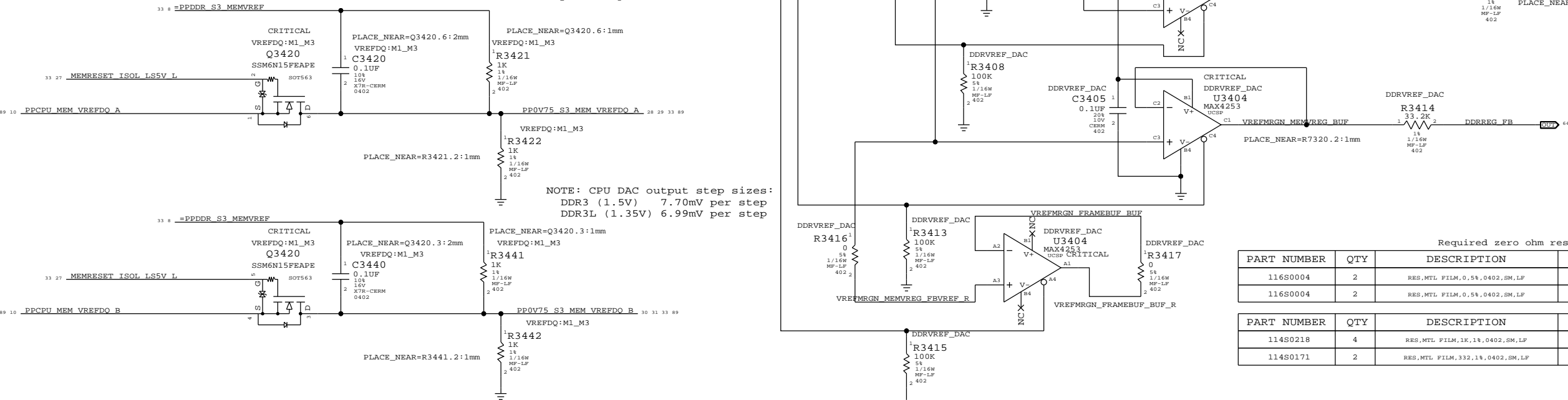
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.000V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

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SYNC DATE=01/13/2012

DDR3/FRAMEBUF VREF MARGINING

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DRAWING NUMBER 051-9589

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PAGE 34 OF 132

SHEET 33 OF 99

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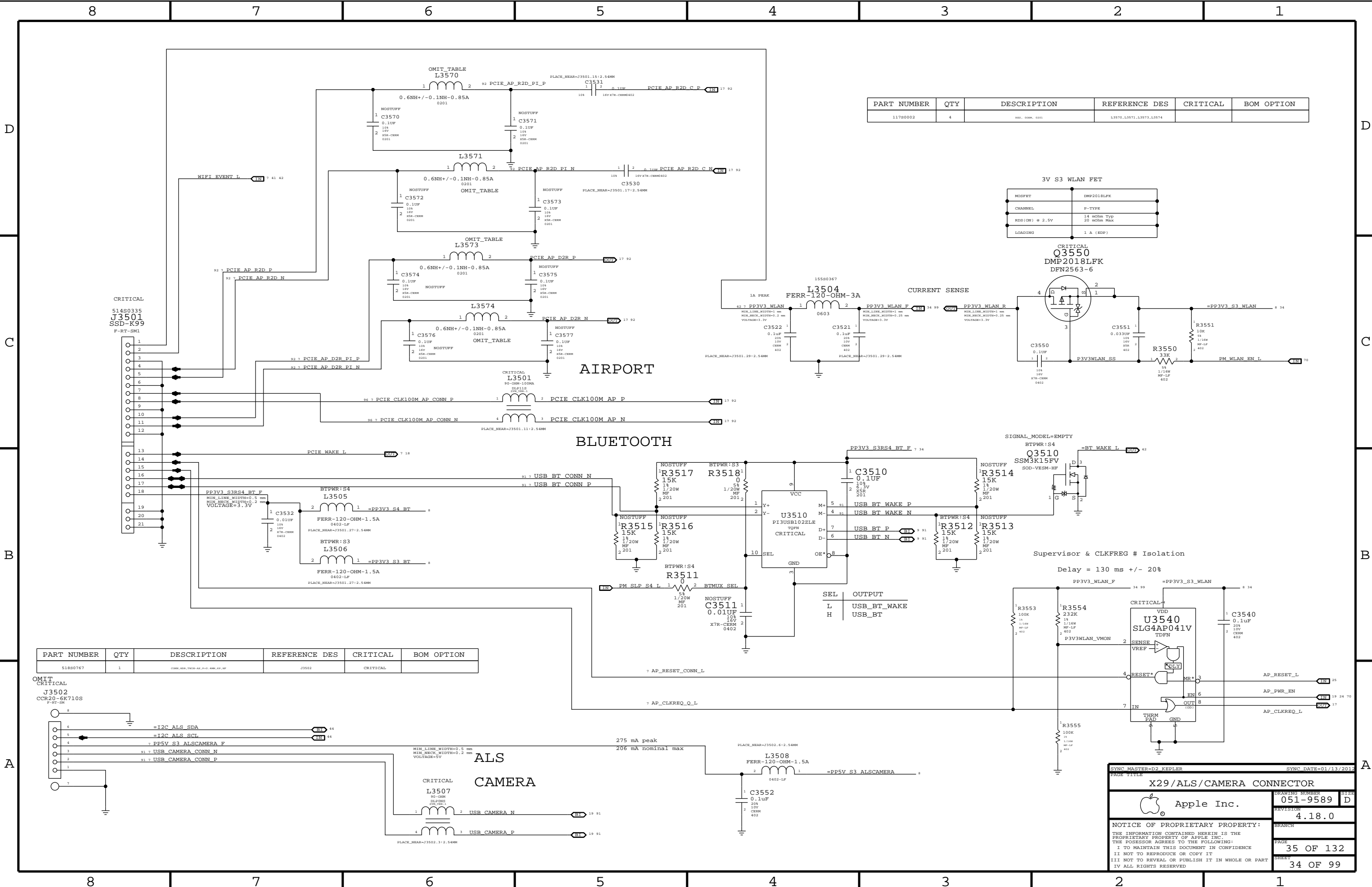
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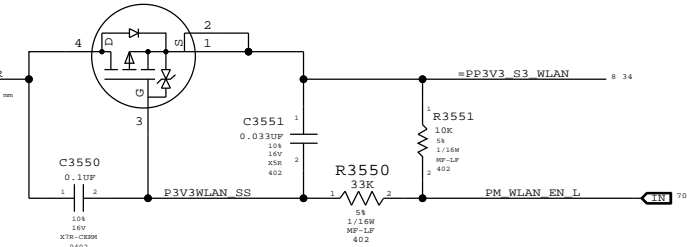
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	4	880, 000M, 0201	L3570, L3571, L3573, L3574		

3V S3 WLAN FET	
MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON) @ 2.5V	14 mOhm Typ 20 mOhm Max
LOADING	1 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6



AIRPORT

BLUETOOTH

SIGNAL_MODEL=EMPTY

BTMPWR:S4

Q3510

SSM3K15FV

SOD-VESM-HF

BT WAKE L

BT WAKE P

BT WAKE N

BT WAKE S

BT WAKE T

BT WAKE U

BT WAKE V

BT WAKE W

BT WAKE X

BT WAKE Y

BT WAKE Z

BT WAKE A

BT WAKE B

BT WAKE C

BT WAKE D

BT WAKE E

BT WAKE F

BT WAKE G

BT WAKE H

BT WAKE I

BT WAKE J

BT WAKE K

BT WAKE L

BT WAKE M

BT WAKE N

BT WAKE O

BT WAKE P

BT WAKE Q

BT WAKE R

BT WAKE S

BT WAKE T

BT WAKE U

BT WAKE V

BT WAKE W

BT WAKE X

BT WAKE Y

BT WAKE Z

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BT WAKE R

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BT WAKE U

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BT WAKE X

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BT WAKE A

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BT WAKE R

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BT WAKE X

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BT WAKE A

BT WAKE B

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BT WAKE X

BT WAKE Y

BT WAKE Z

BT WAKE A

BT WAKE B

BT WAKE C

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BT WAKE J

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BT WAKE T

BT WAKE U

BT WAKE V

BT WAKE W

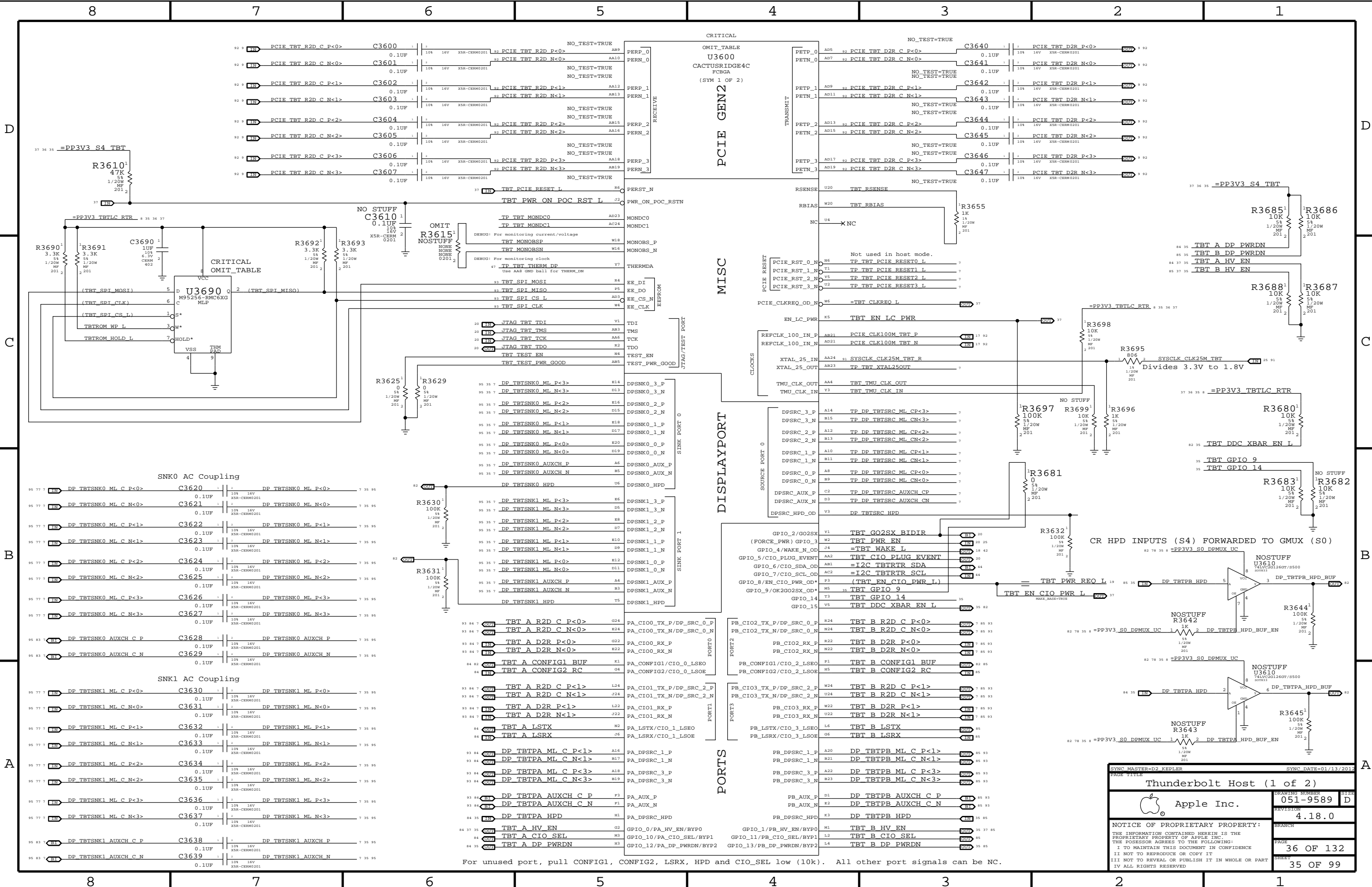
BT WAKE X

BT WAKE Y

BT WAKE Z

BT WAKE A

BT WAKE B



SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER

051-9589

SIZE

D

REVISION

4.18.0

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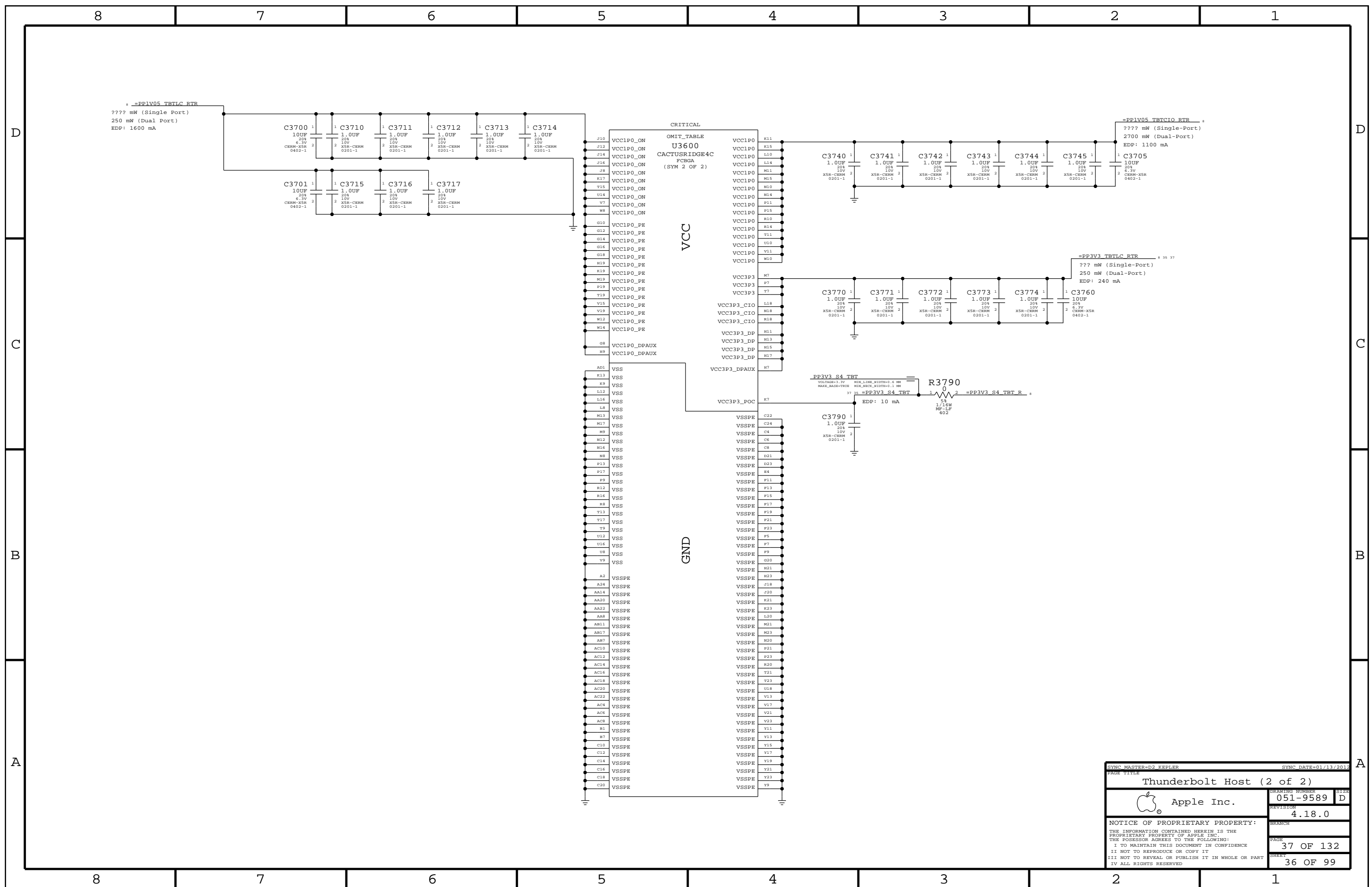
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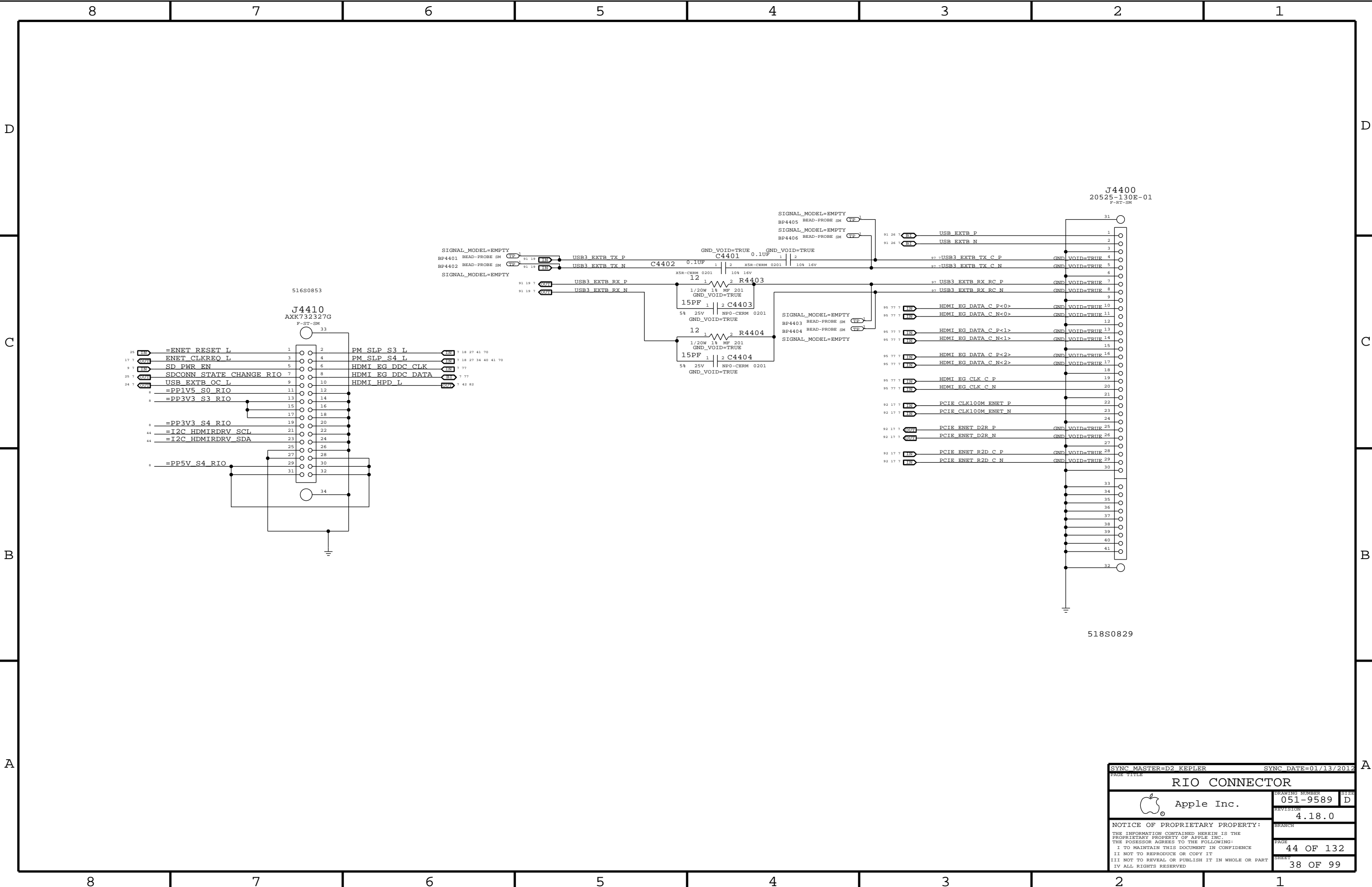
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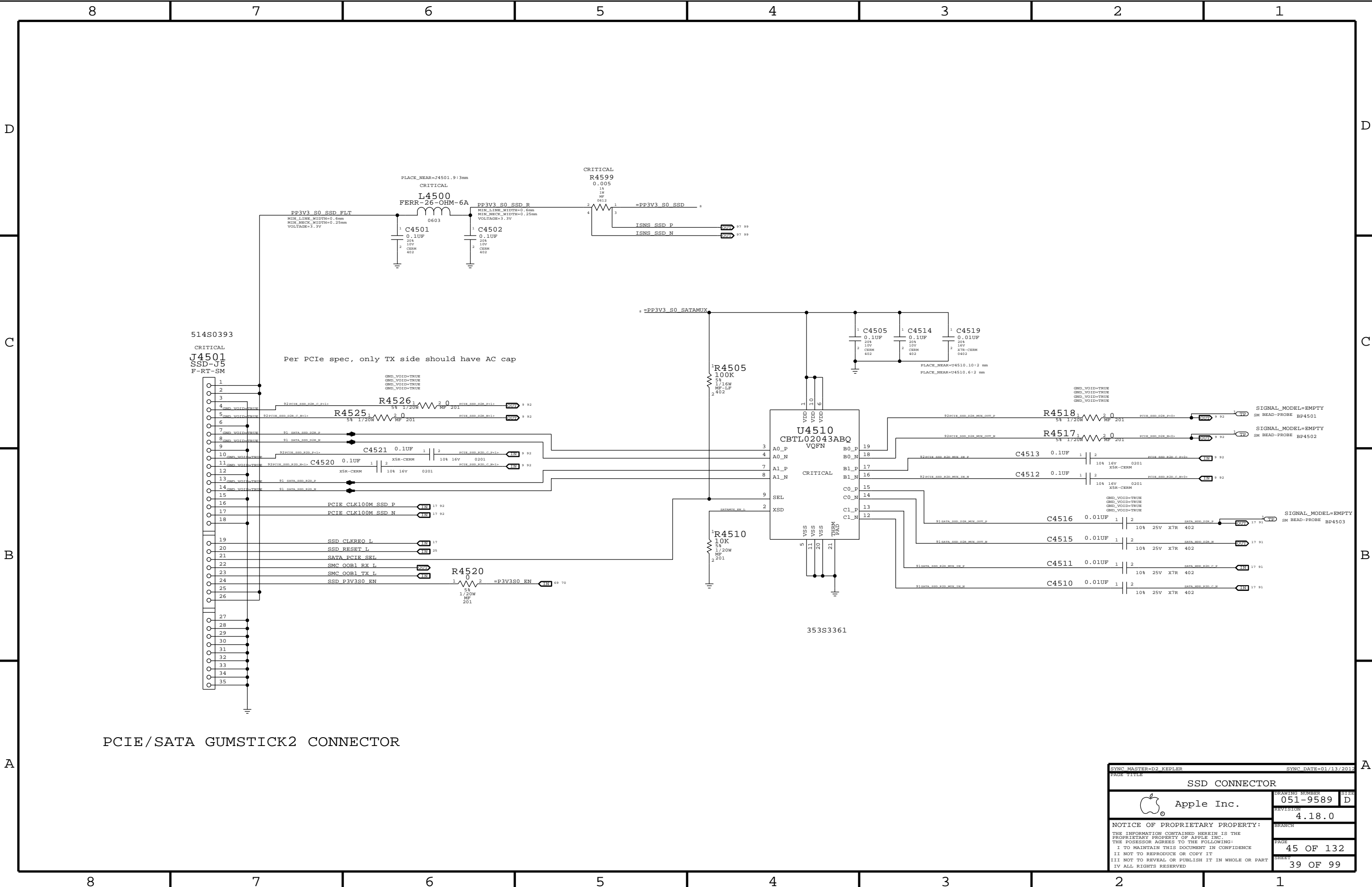
36 OF 132

SHEET


35 OF 99



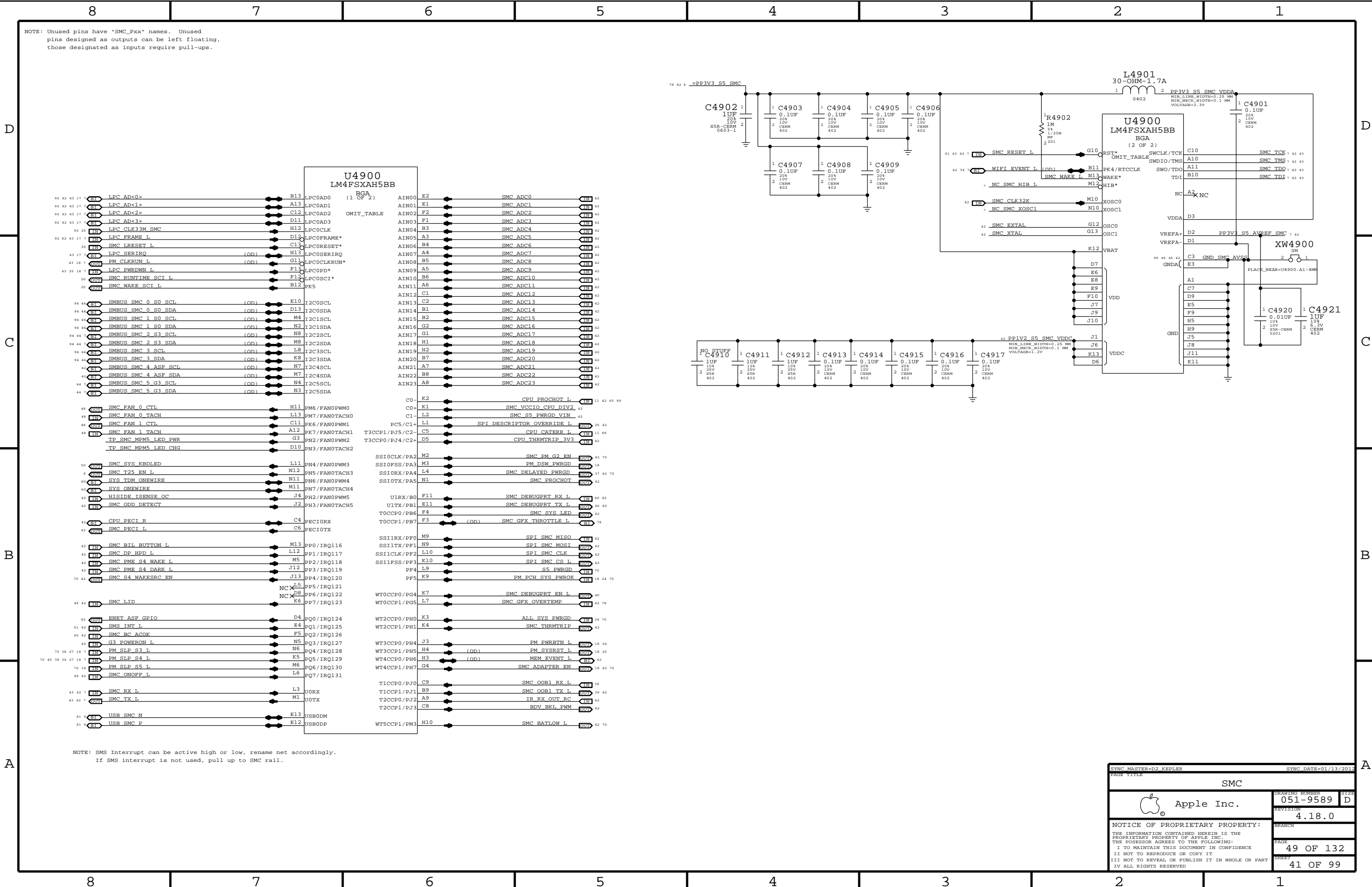


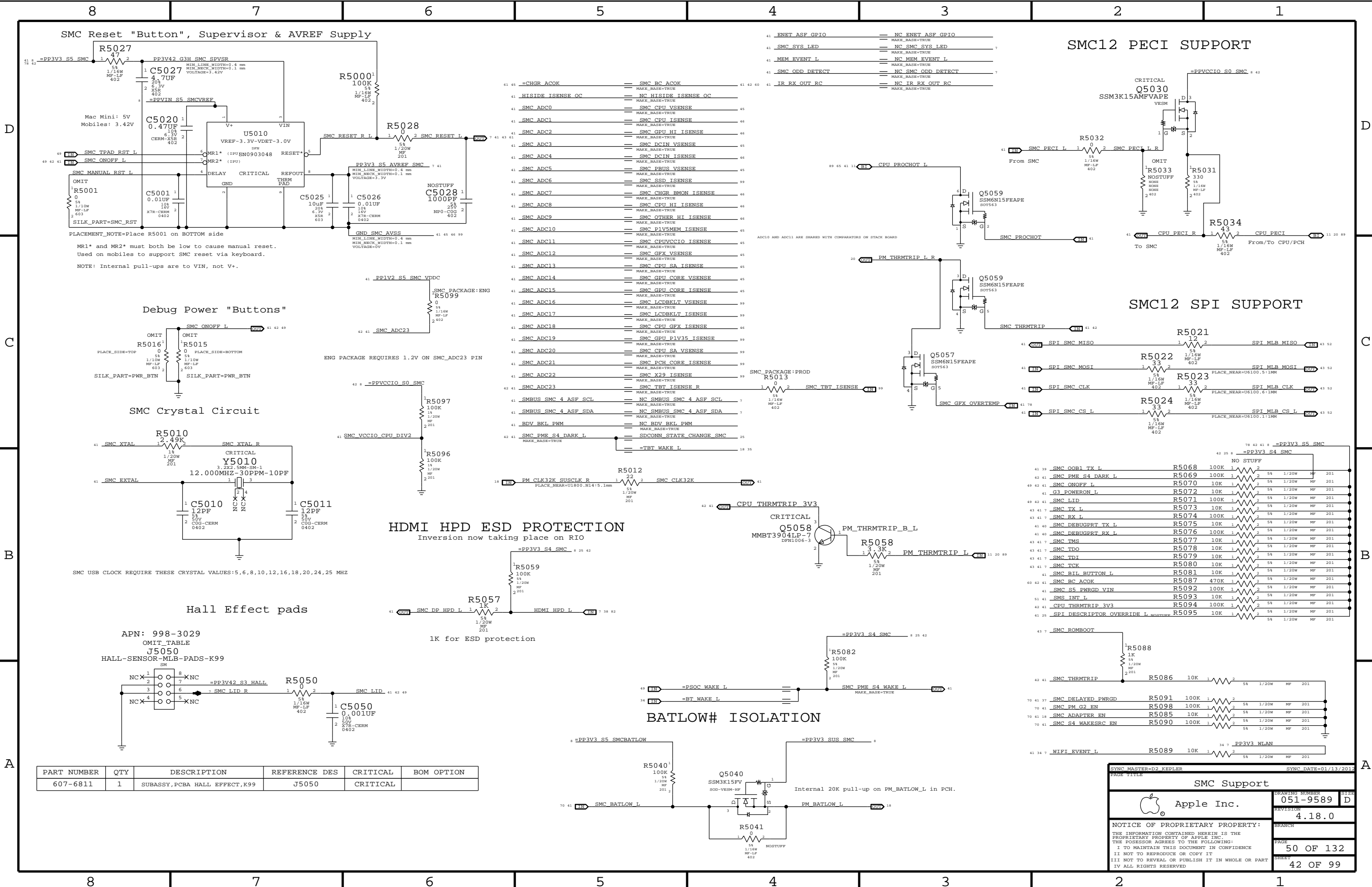


PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
SSD CONNECTOR			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
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		SHEET	39 OF 99







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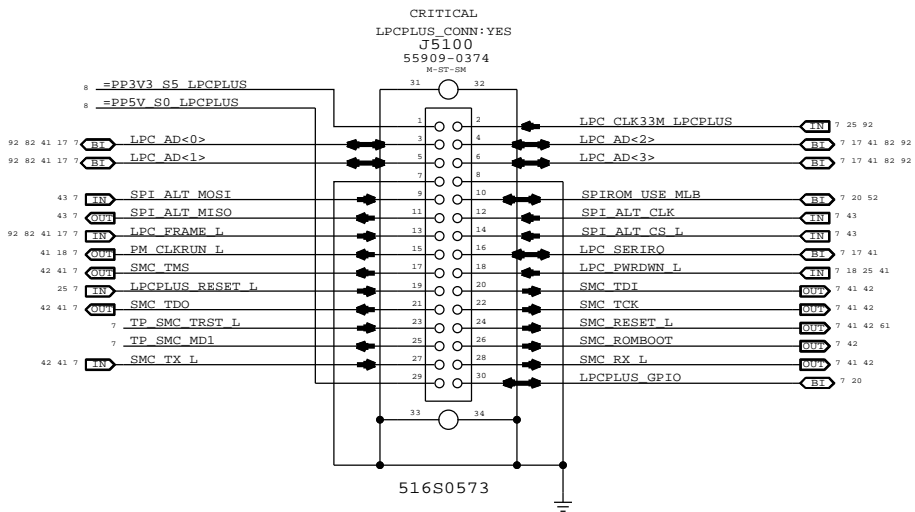
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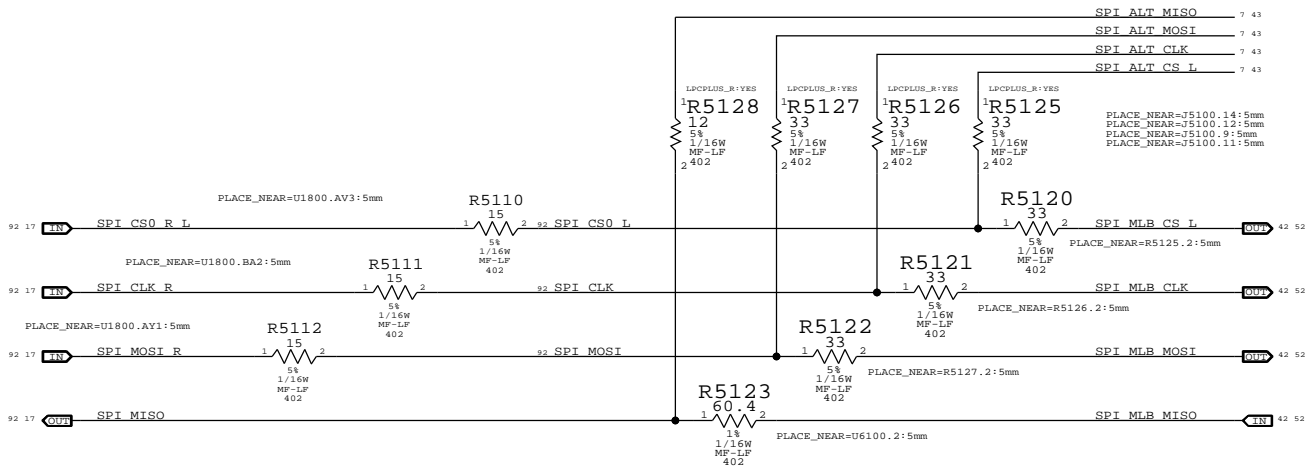
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
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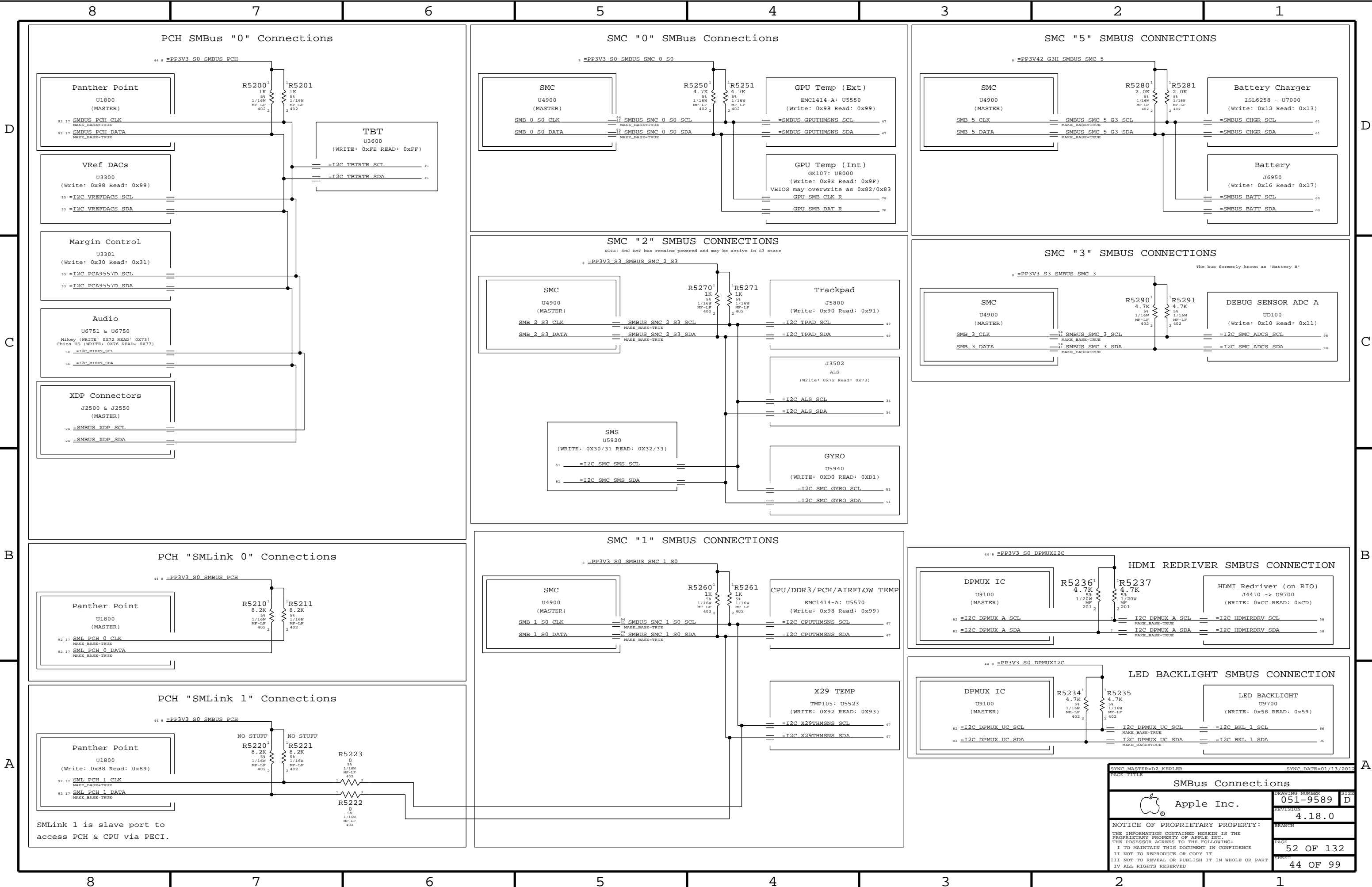
LPC+SPI Connector

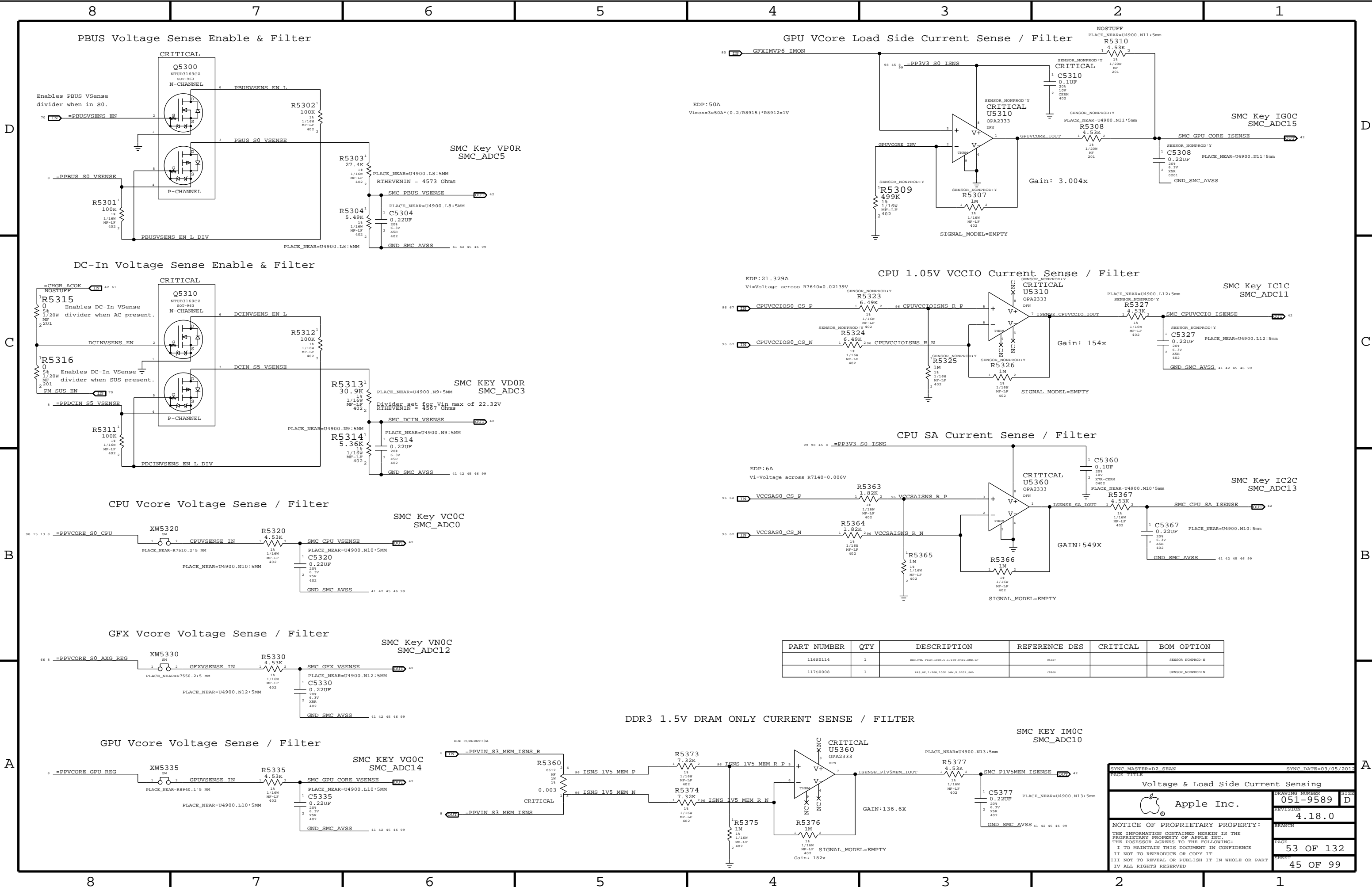


SPI Bus Series Termination



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9589		D
	REVISION		PAGE
4.18.0		51 OF 132	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	1	RES,HTL, 0.125W, 100K, 0.1/16W, 0.402, 402, LF	C5127		SENSOR_NONPROD:Y
11780008	1	RES,MP, 1/20W, 100K, 0.1/16W, 0.402, 402, LF	C5128		SENSOR_NONPROD:Y

SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

Voltage & Load Side Current Sensing

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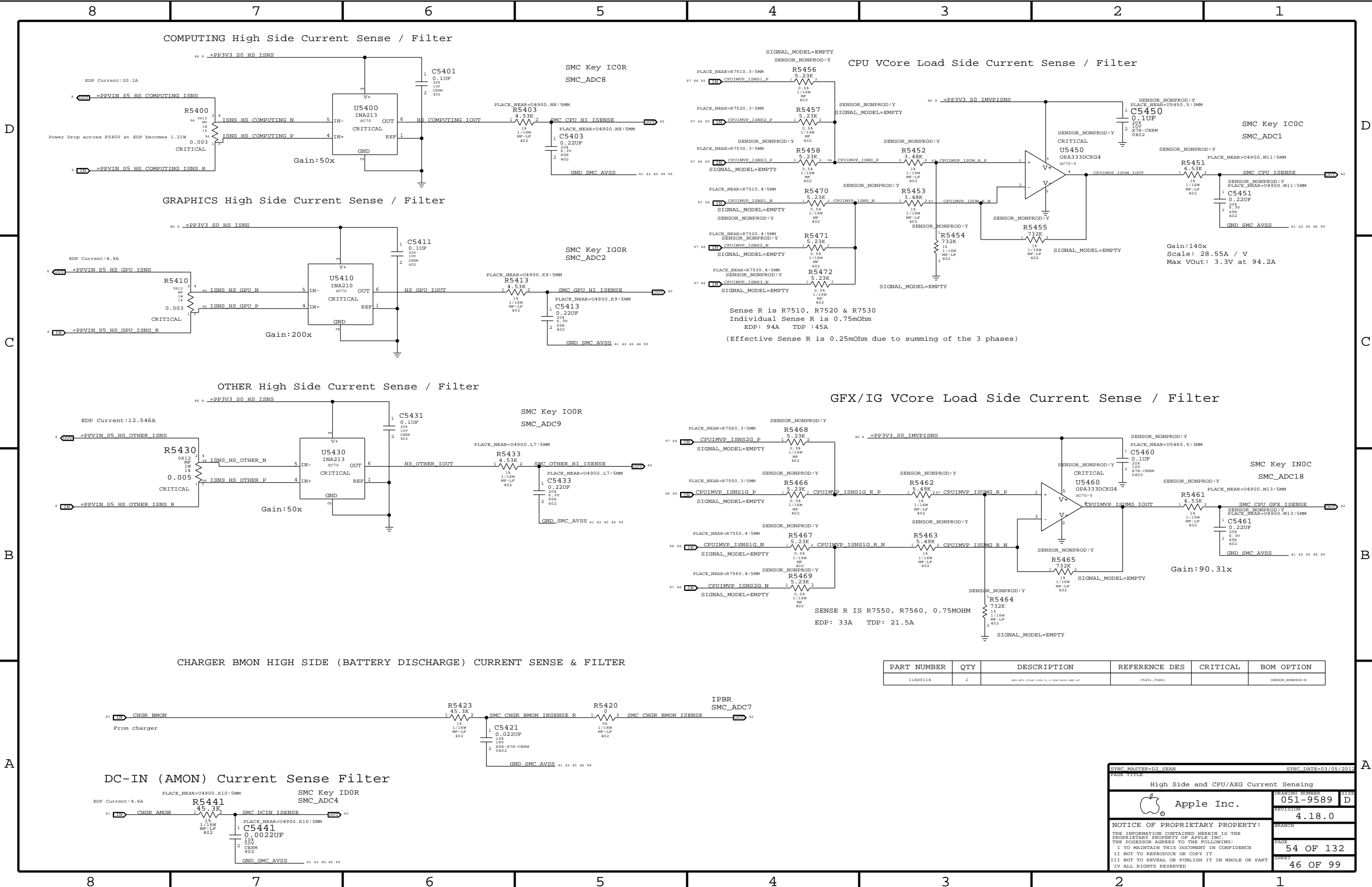
4.18.0

PAGE

53 OF 132

SHEET

45 OF 99




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	2	RES,MTL,PT100,100K,5,1/16W,0402,080D,LF	C5451,C5461		SENSOR_NONPROD:N

SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

High Side and CPU/AXG Current Sensing

 Apple Inc.

DRAWING NUMBER
051-9589

REVISION
4.18.0

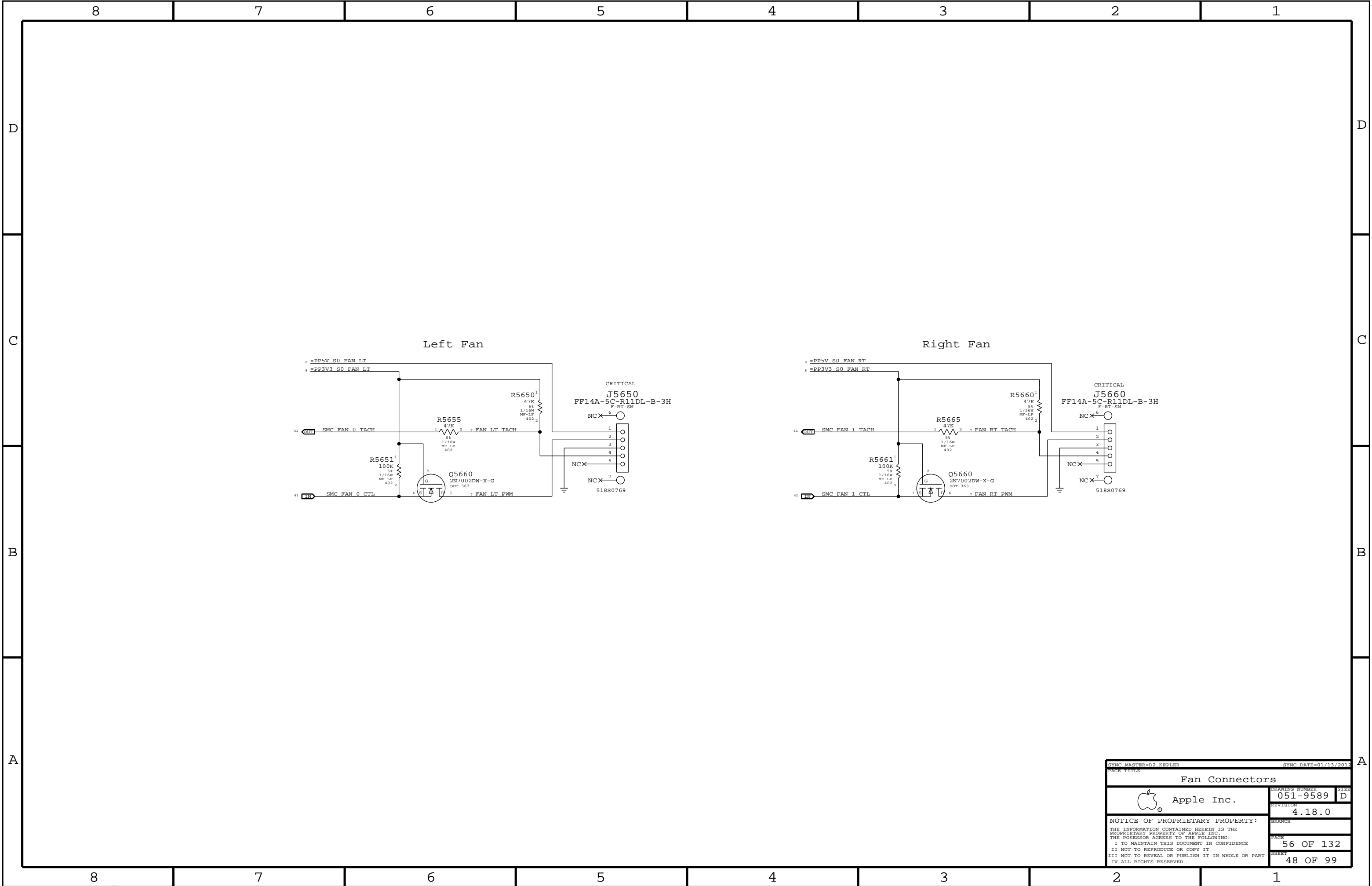
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PAGE
54 OF 132

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46 OF 99

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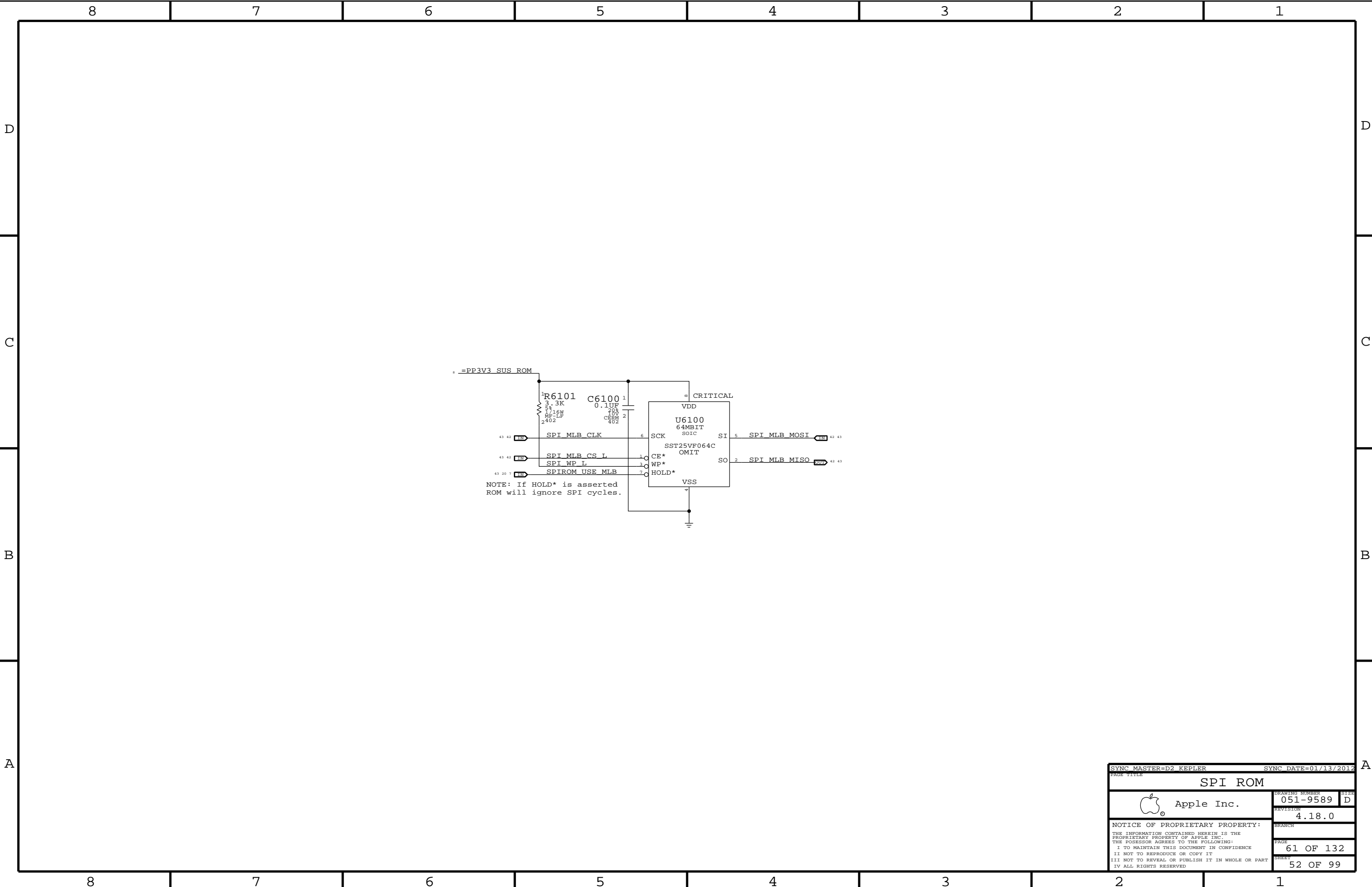



- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

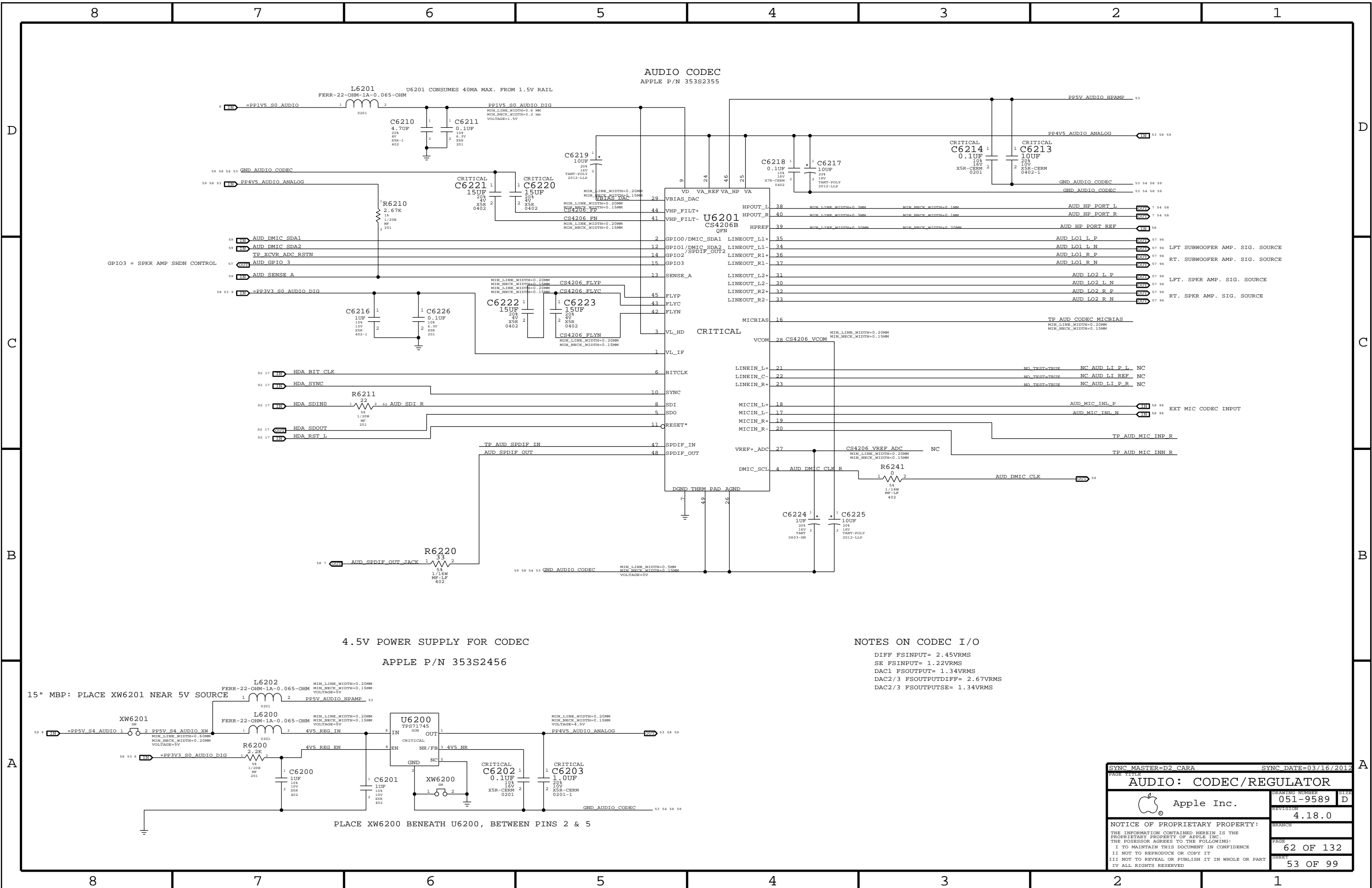
IPD Flex Connector

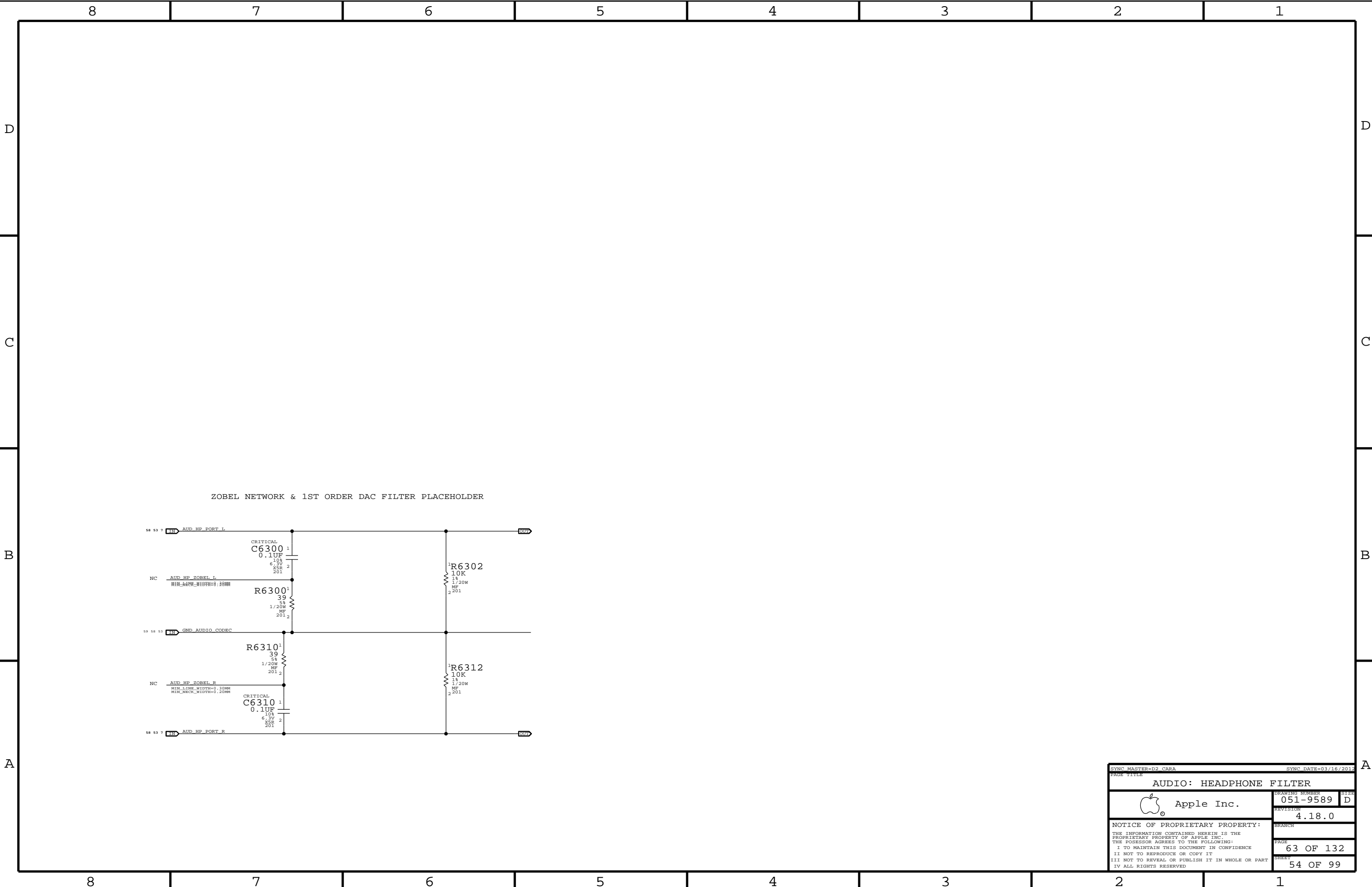
CRITICAL




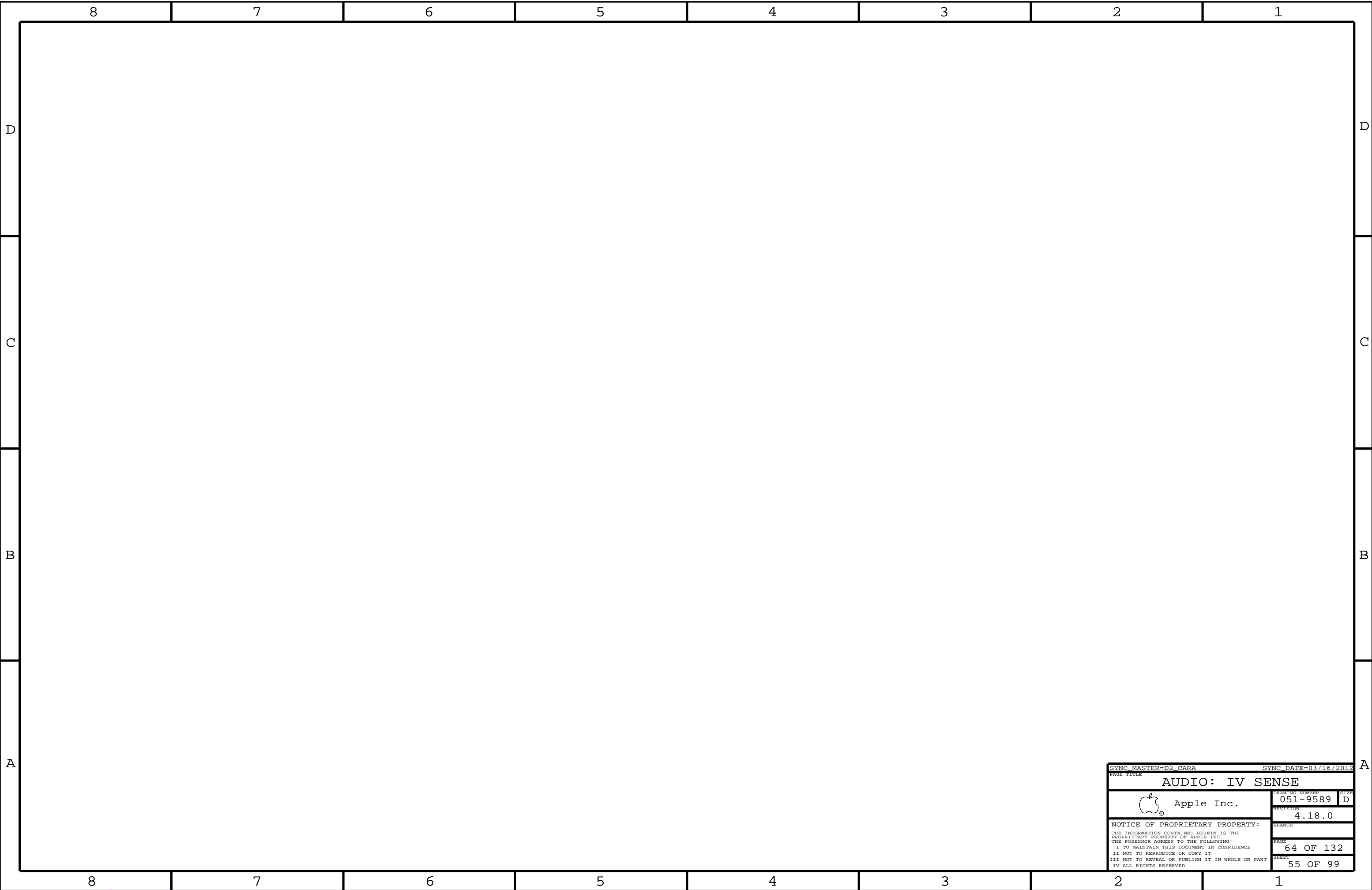


SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
SPI ROM			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
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PAGE		61 OF 132	
SHEET		52 OF 99	






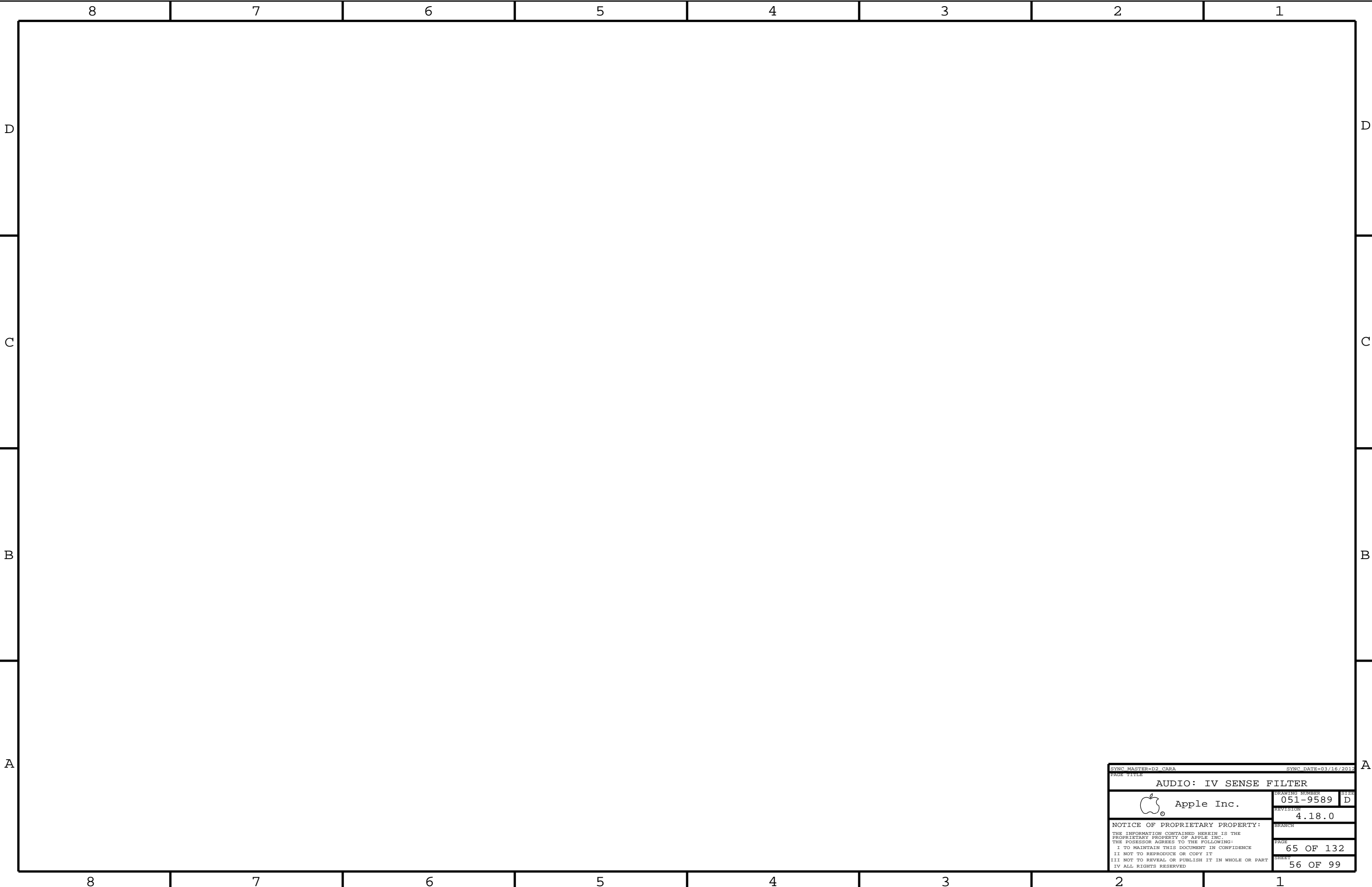
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 Apple Inc.		DRAWING NUMBER	051-9589
		REVISION	4.18.0
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		PAGE	63 OF 132
		SHEET	54 OF 99



SYNC MASTER=D2_CARA

SYNC DATE=03/16/2012


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		PAGE	64 OF 132
		SHEET	55 OF 99



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AUDIO: IV SENSE FILTER

 Apple Inc.

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051-9589

REVISION
4.18.0

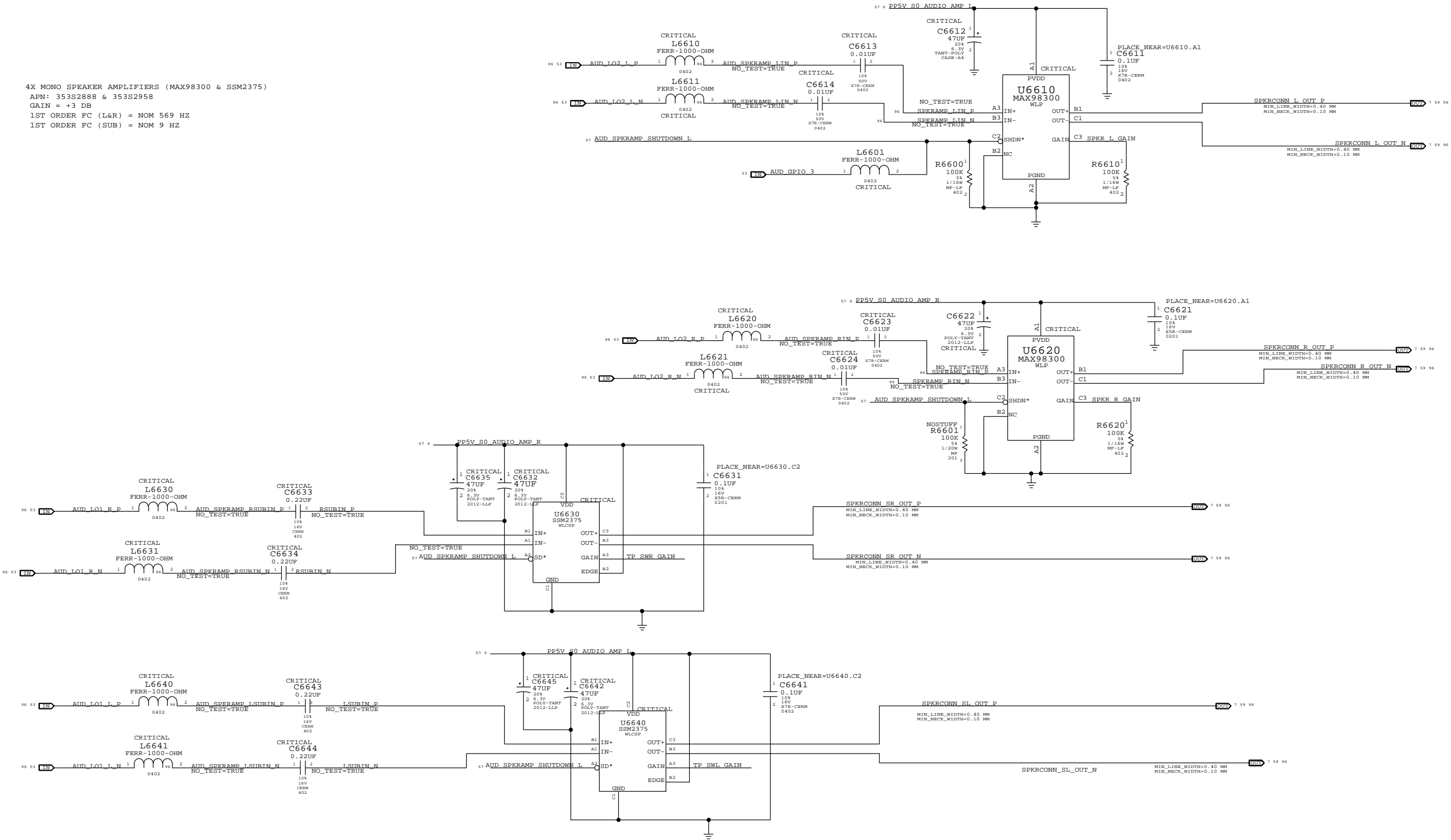
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PAGE
65 OF 132

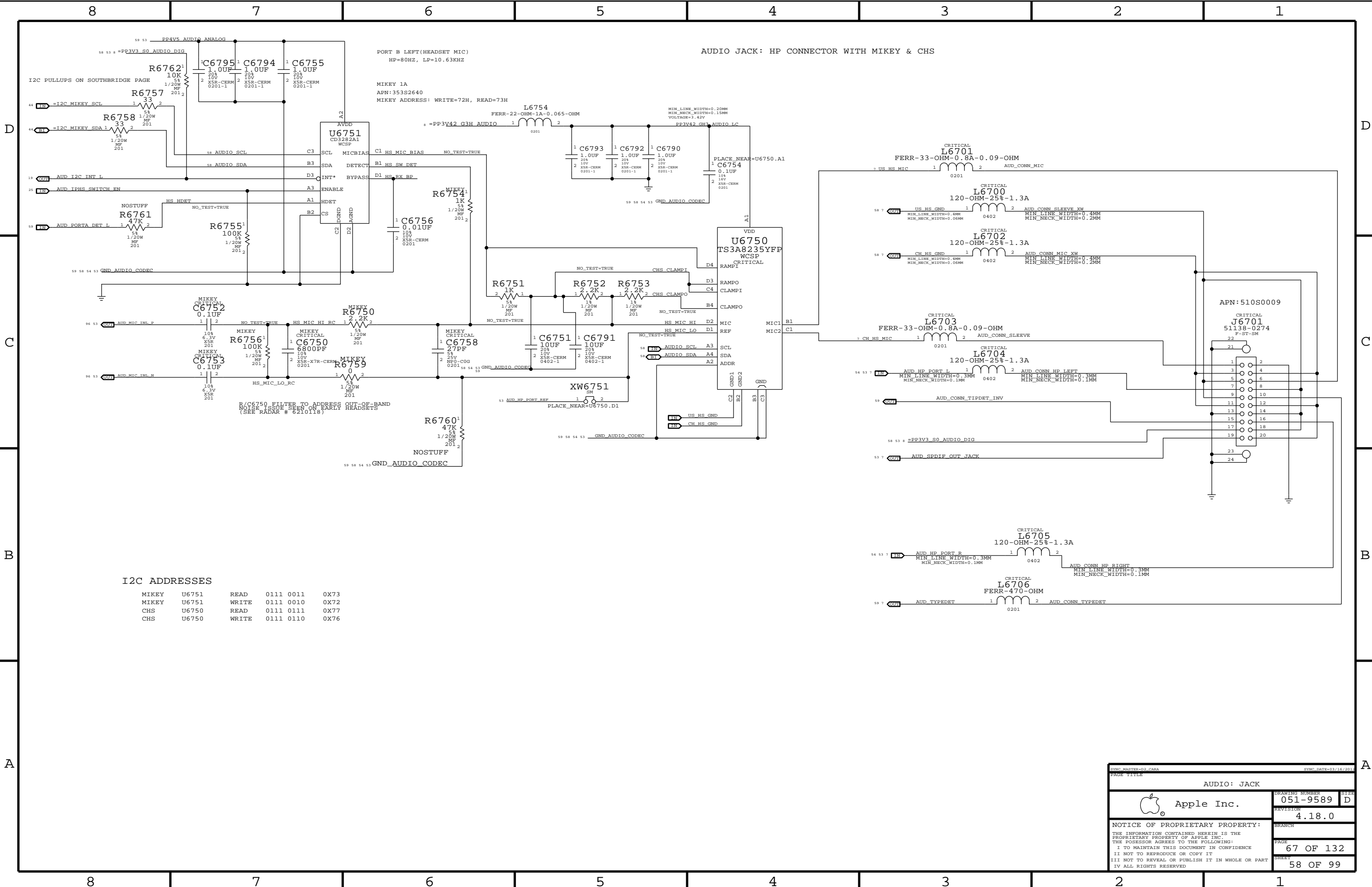
SHEET
56 OF 99

SIZE
D

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=D2 CARA		SYNC DATE=03/16/2012	
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I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

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SYNC: DATE=03/16/2015

AUDIO: JACK

 Apple Inc.

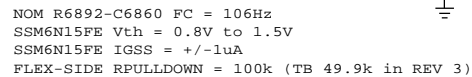
051-9589


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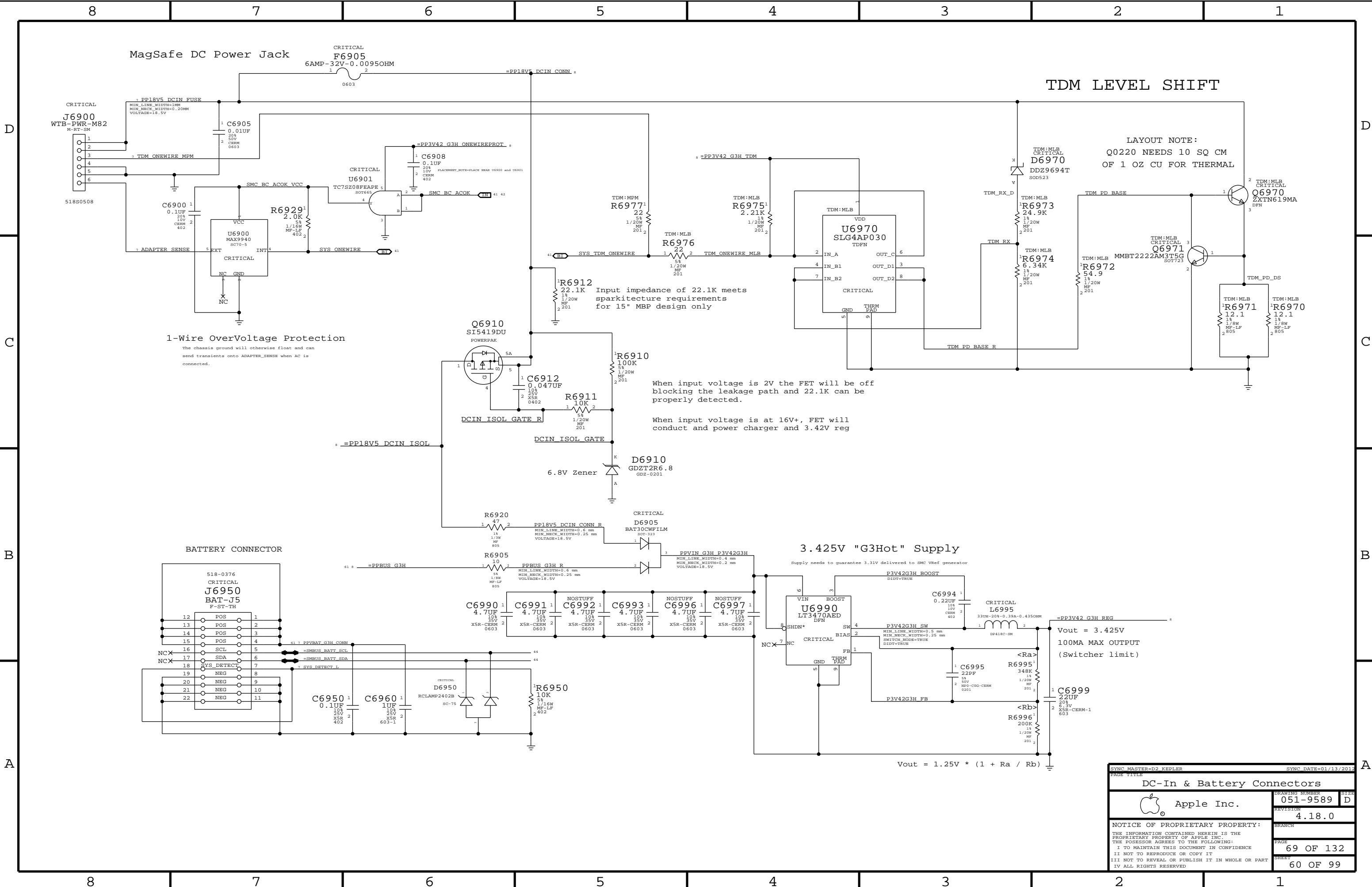
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
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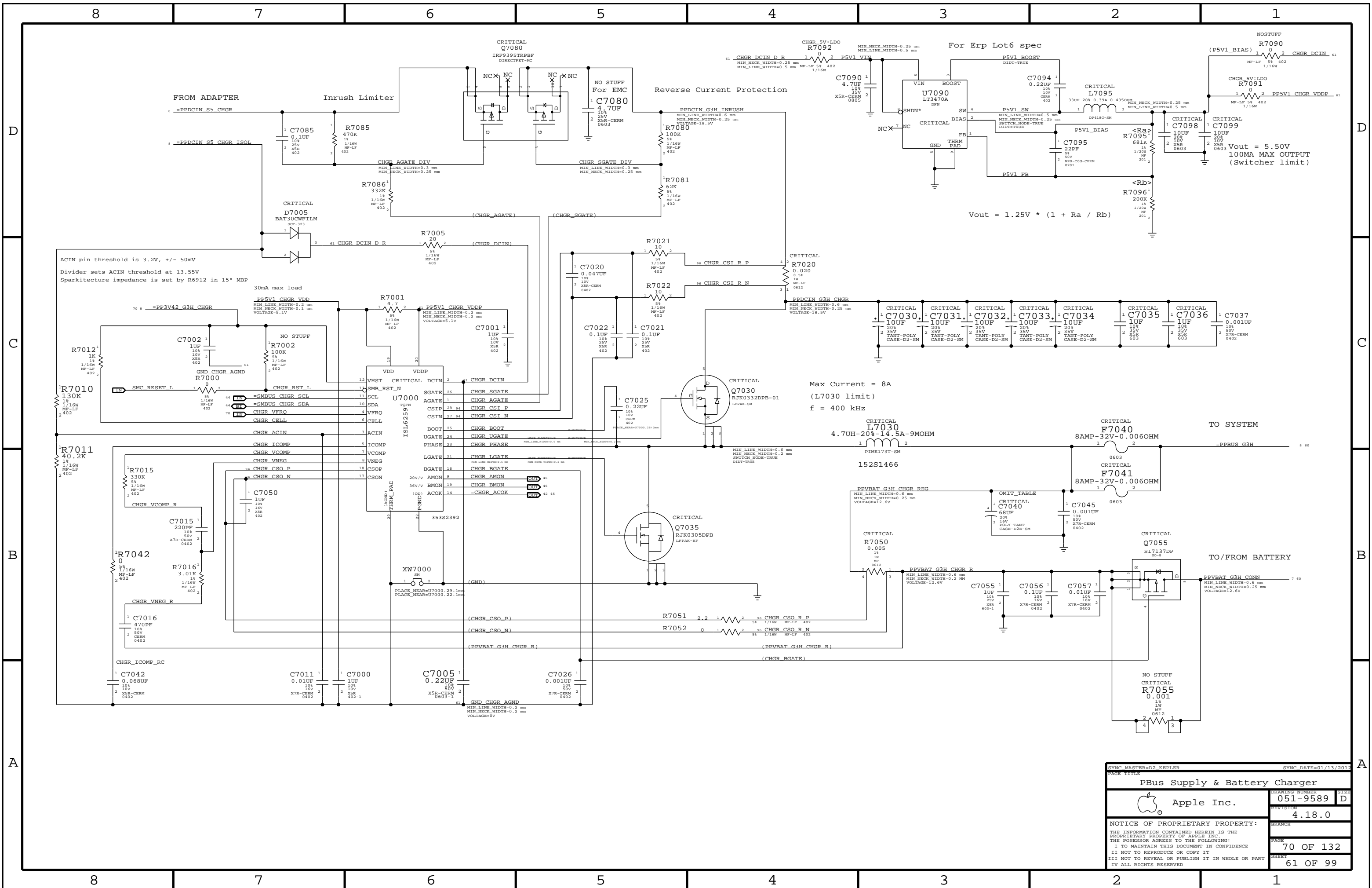
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


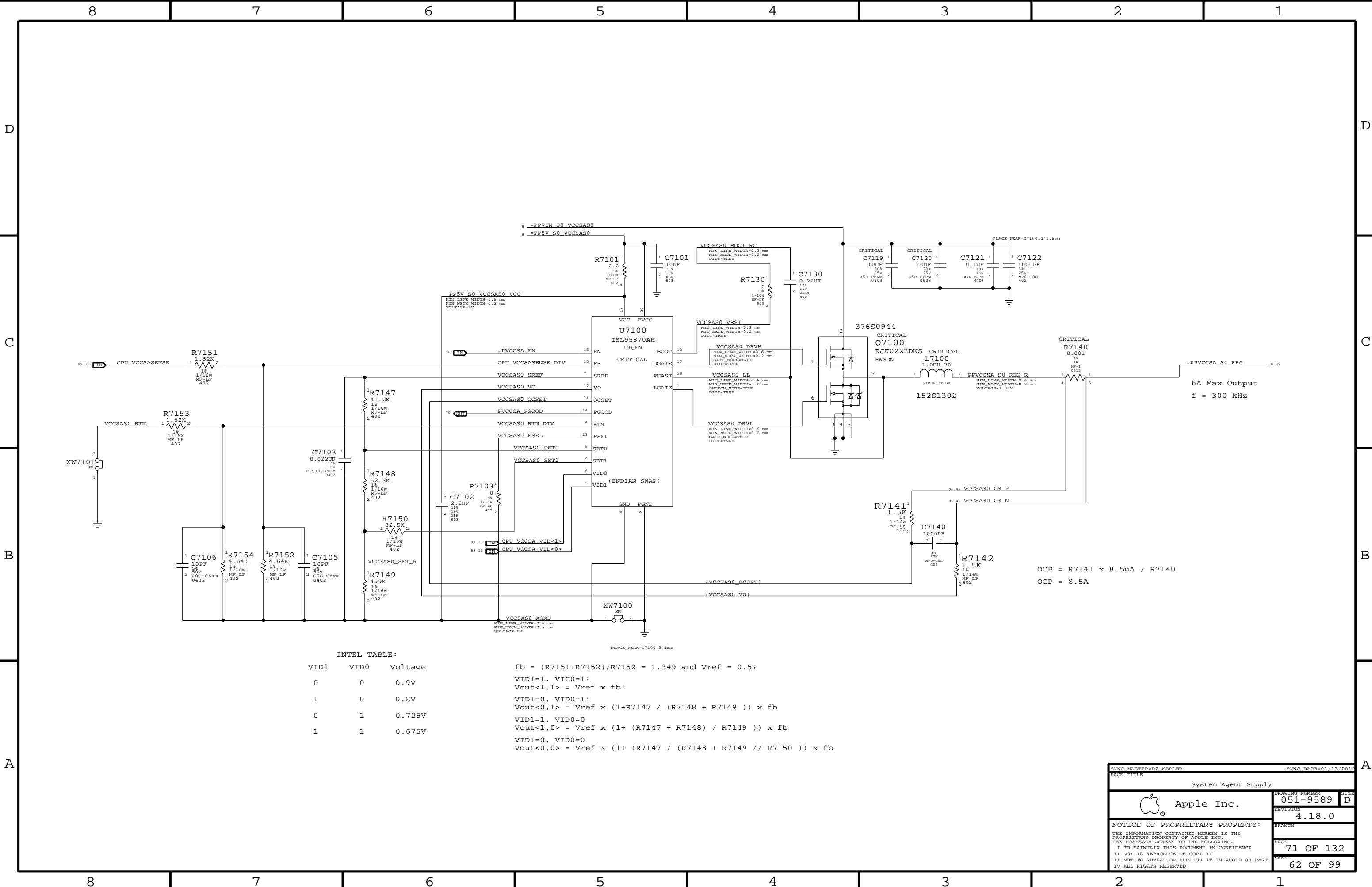
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 Apple Inc.		DRAWING NUMBER	
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		BRANCH	
		PAGE	
		68 OF 132	
		SHEET	
		59 OF 99	

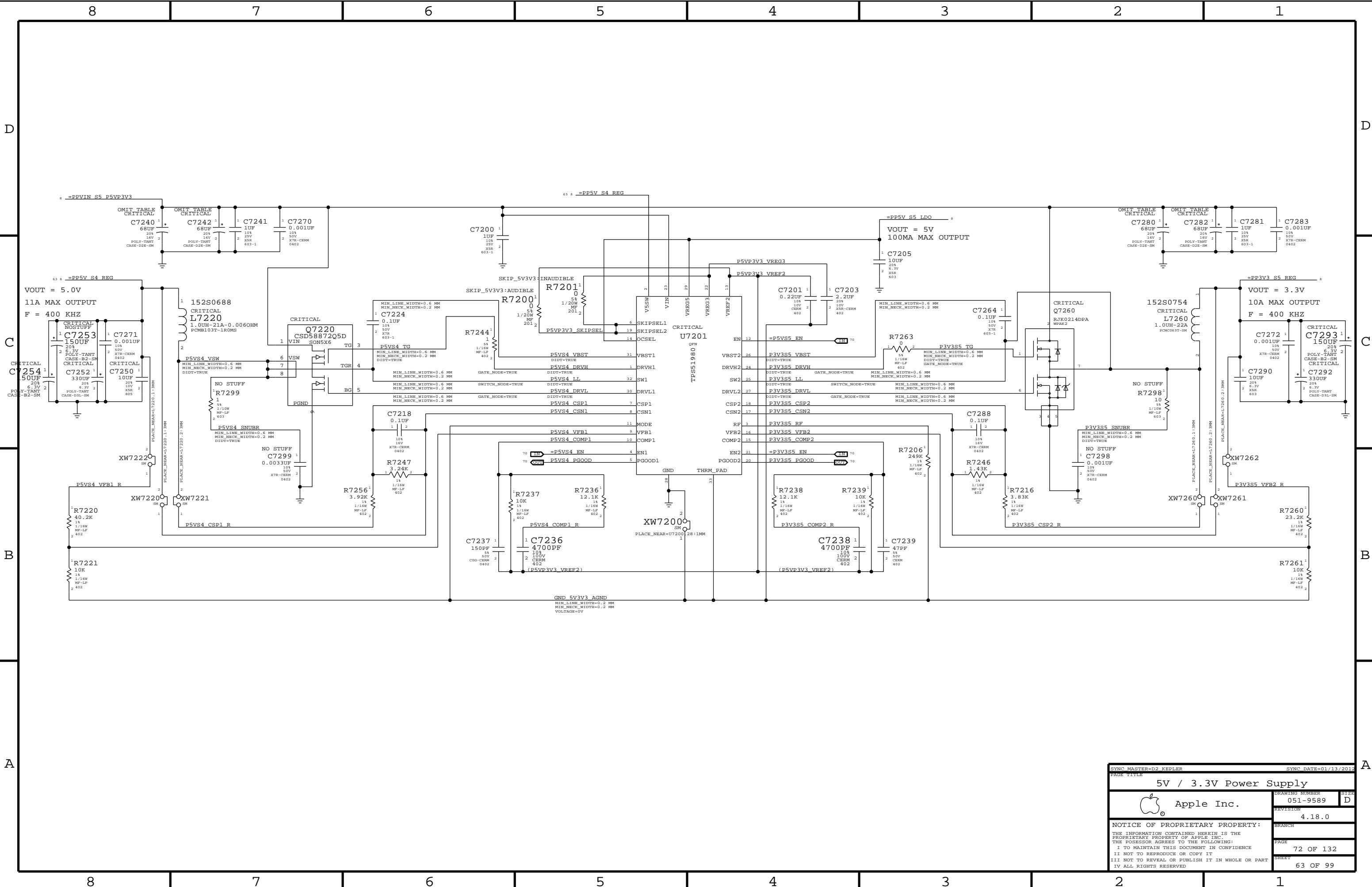



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
DC-In & Battery Connectors		DRAWING NUMBER	
 Apple Inc.		051-9589	D
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		4.18.0	
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		69 OF 132	
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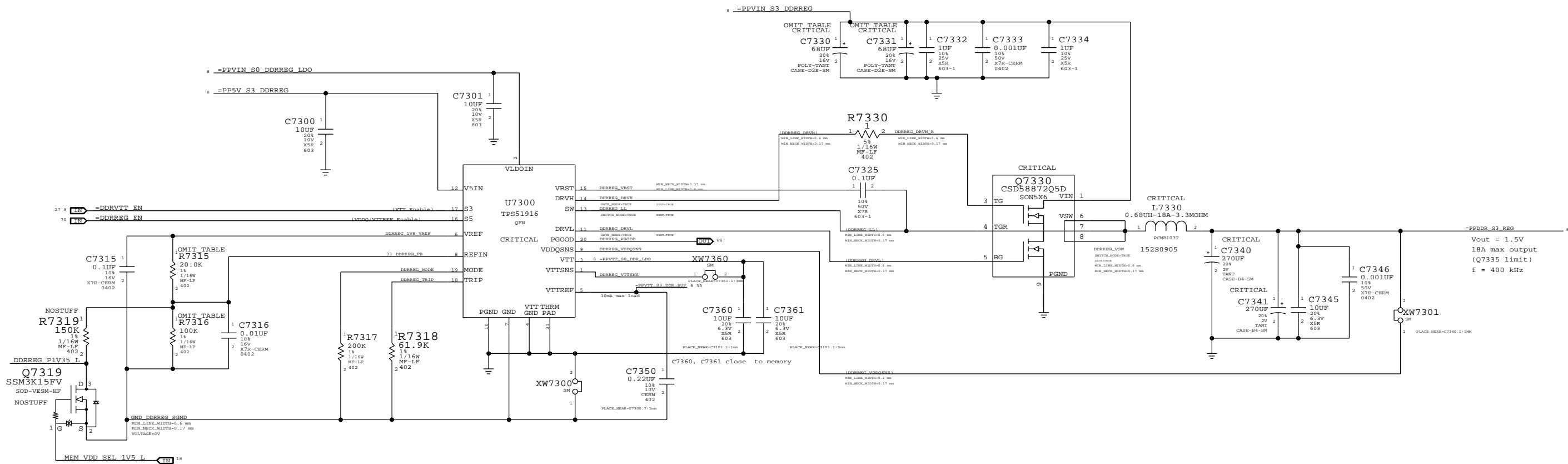
SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	70 OF 132
		SHEET	61 OF 99





SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
5V / 3.3V Power Supply		DRAWING NUMBER	
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		BRANCH	
		PAGE	72 OF 132
		SHEET	63 OF 99

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES,MTL,P10M,1/5W,20.0K,1,0402,080,LP	R7315		PPDDR:1V5
114S0342	1	RES,MTL,P10M,1/5W,19.6K,1,0402,080,LP	R7315		PPDDR:1V35
114S0411	1	RES,MTL,P10M,1/5W,100K,1,0402,080,LP	R7316		PPDDR:1V5
114S0389	1	RES,MTL,P10M,1/5W,57.6K,1,0402,080,LP	R7316		PPDDR:1V35

DRAWING NUMBER		051-9589	SIZE	D
REVISION		4.18.0		
BRANCH				
PAGE		73 OF 132		
SHEET		64 OF 99		

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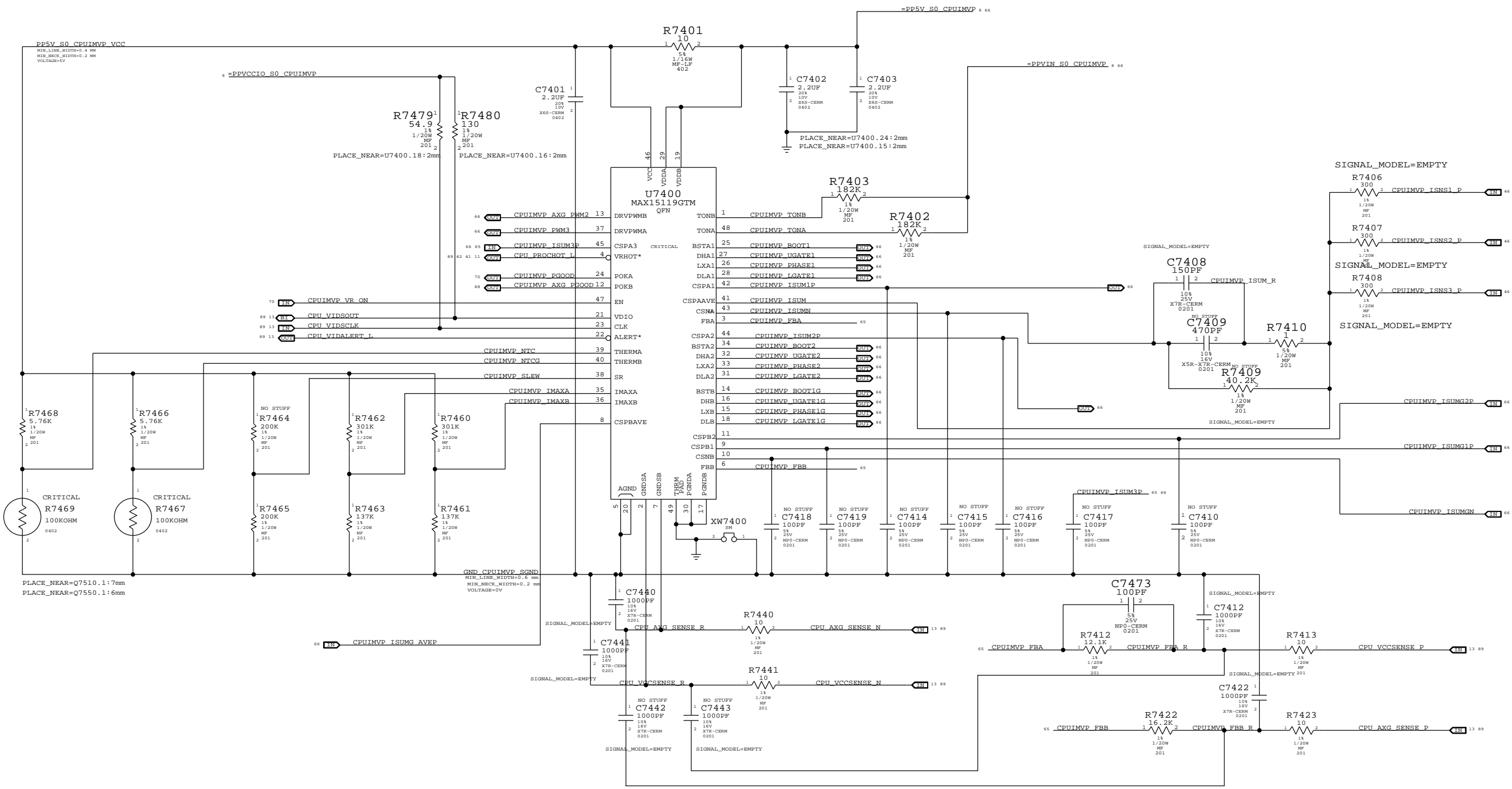
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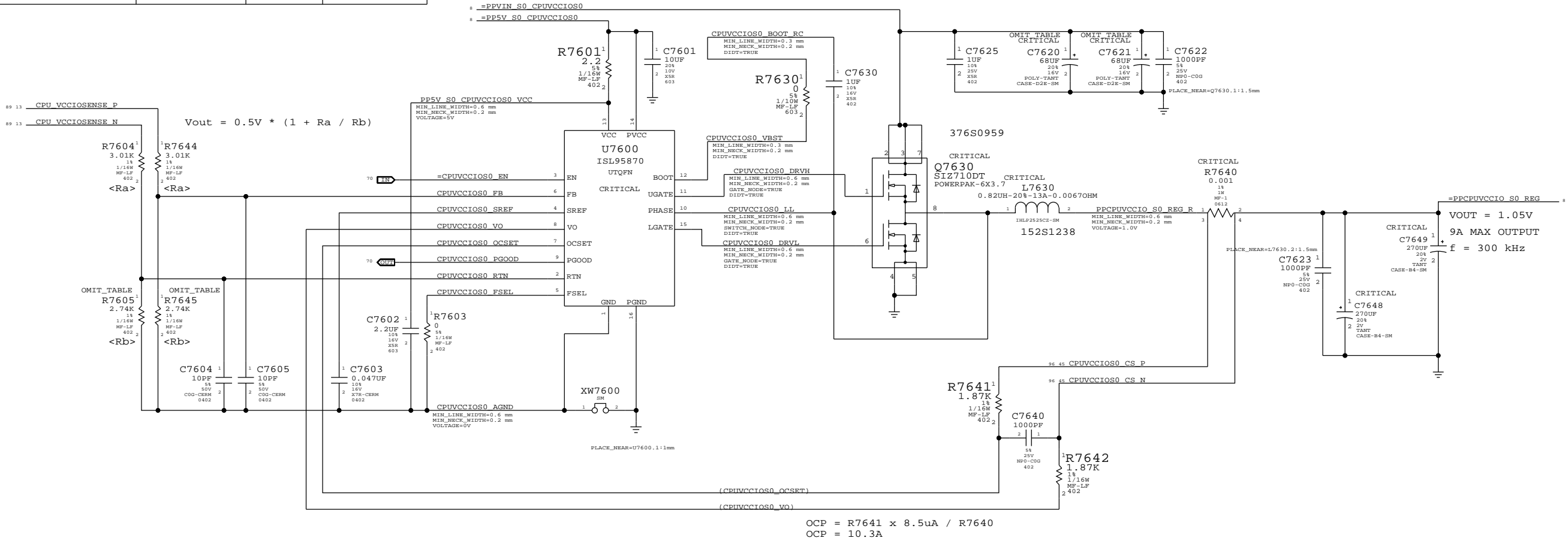



SYNOPSIS: CPU IMVP7 & AXG VCore Regulator		SYNOPSIS: CPU IMVP7 & AXG VCore Regulator	
PAGE TITLE		PAGE TITLE	
CPU IMVP7 & AXG VCore Regulator		CPU IMVP7 & AXG VCore Regulator	
Apple Inc.		Apple Inc.	
DRAWING NUMBER		DRAWING NUMBER	
051-9589		051-9589	
REVISION		REVISION	
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PAGE		PAGE	
74 OF 132		74 OF 132	
SHEET		SHEET	
65 OF 99		65 OF 99	



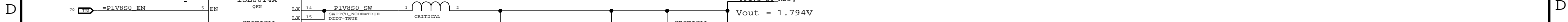
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	REG.MTU.P10M,1/16W,2.74K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	REG.MTU.P10M,1/16W,3.01K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:IVB

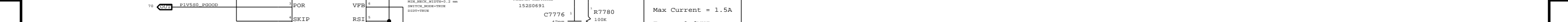
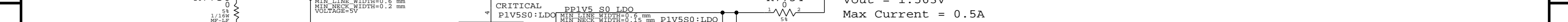


SYMC MASTER-02 KEPLER		SYMC DATE-01/13/2015	
PAGE TITLE			
CPU VCCIO (1V0R1V05 S0) POWER SUPPLY			
 Apple Inc.		DRAWING NUMBER	SIZE
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8	7	6	5	4	3	2	1
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$$V_{out} = 0.8V * (1 + R_a / R_b)$$

[illegible]

A

(
1.0UF
6.3V
2NF
2.2NFB
201.2
 $\langle R_b \rangle$

B

SAMPLE RATE=8KHZ
SYNC MASTER=D2 KEPLER
SYNC DATE=01/13/2013

A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.

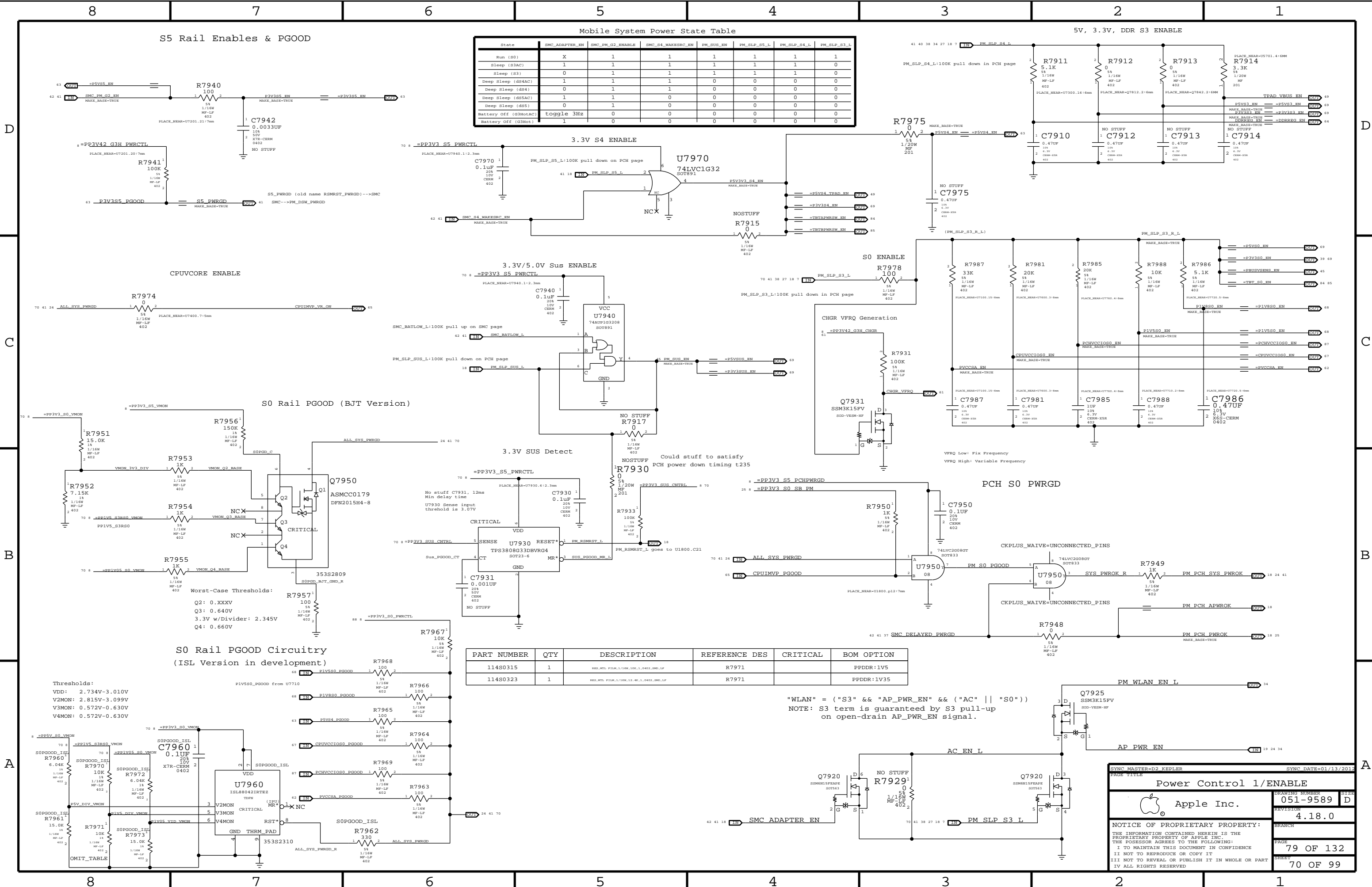


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Mobile System Power State Table							
State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_MAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Deep Sleep (dS4AC)	0	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	1	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES,MTL,P15M,1/16W,10K,1,0402,080,LP	R7971		PPDDR:1V5
114S0323	1	RES,MTL,P15M,1/16W,12.4K,1,0402,080,LP	R7971		PPDDR:1V35

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Power Control 1/ENABLE

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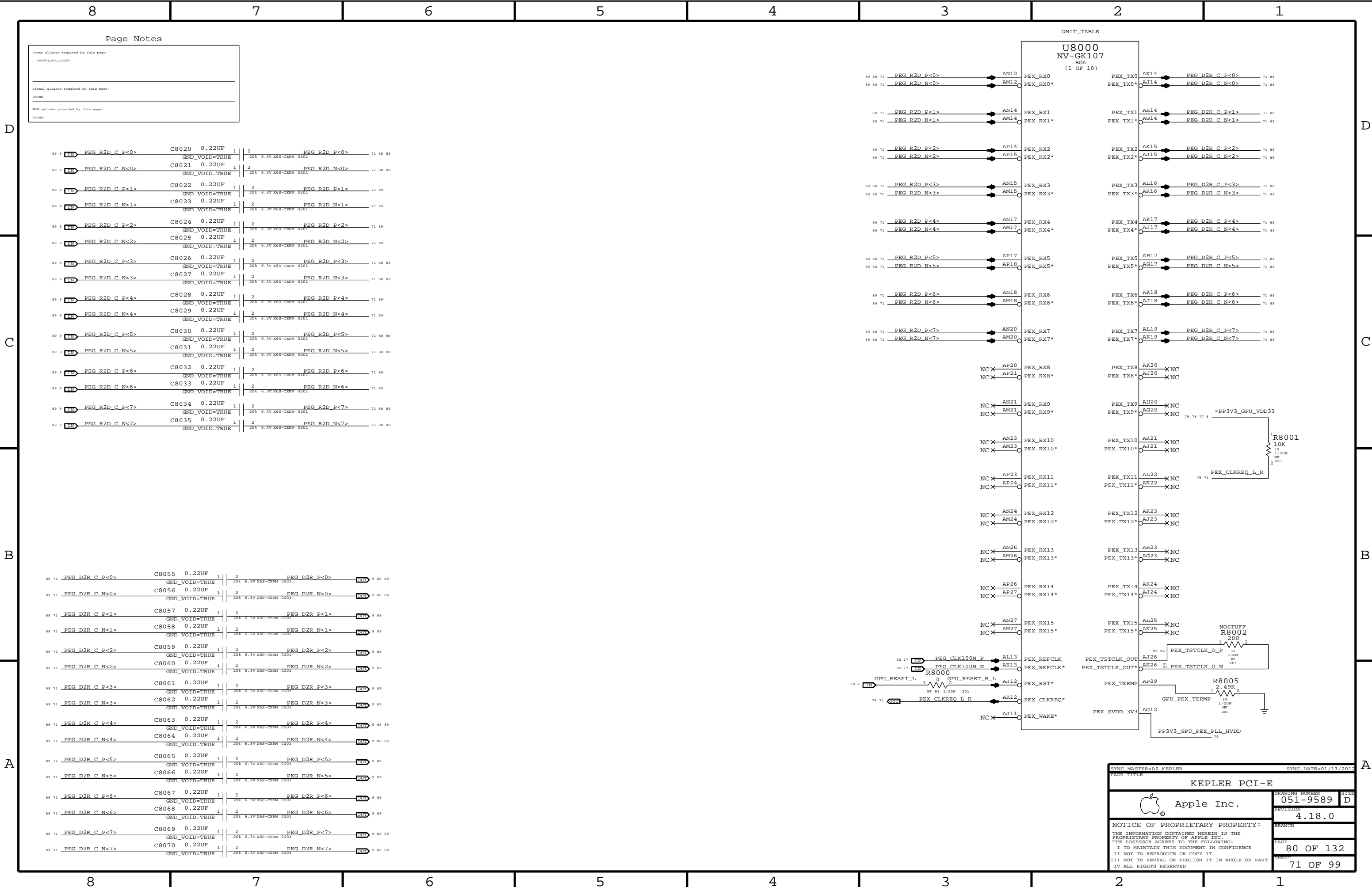
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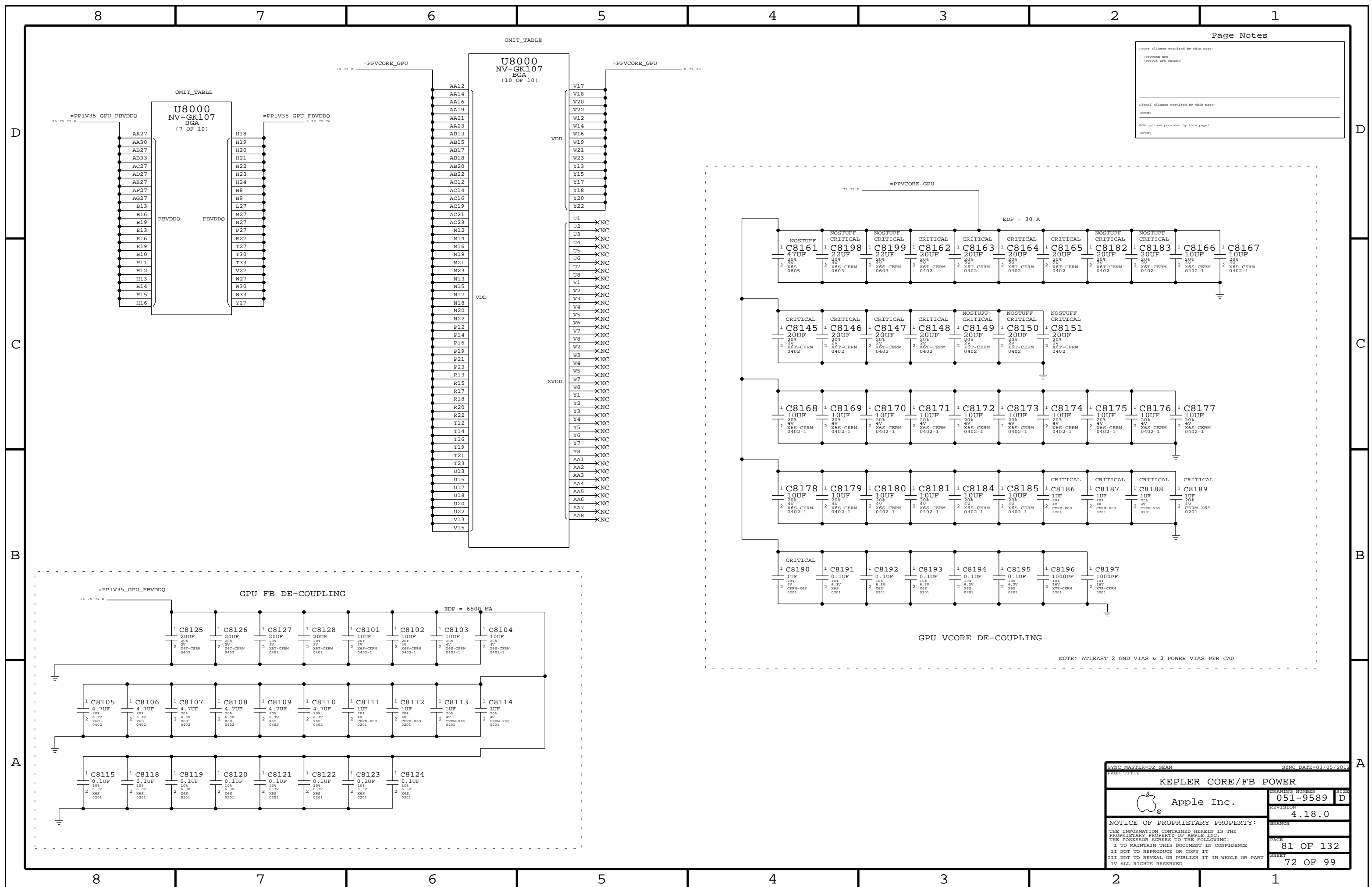
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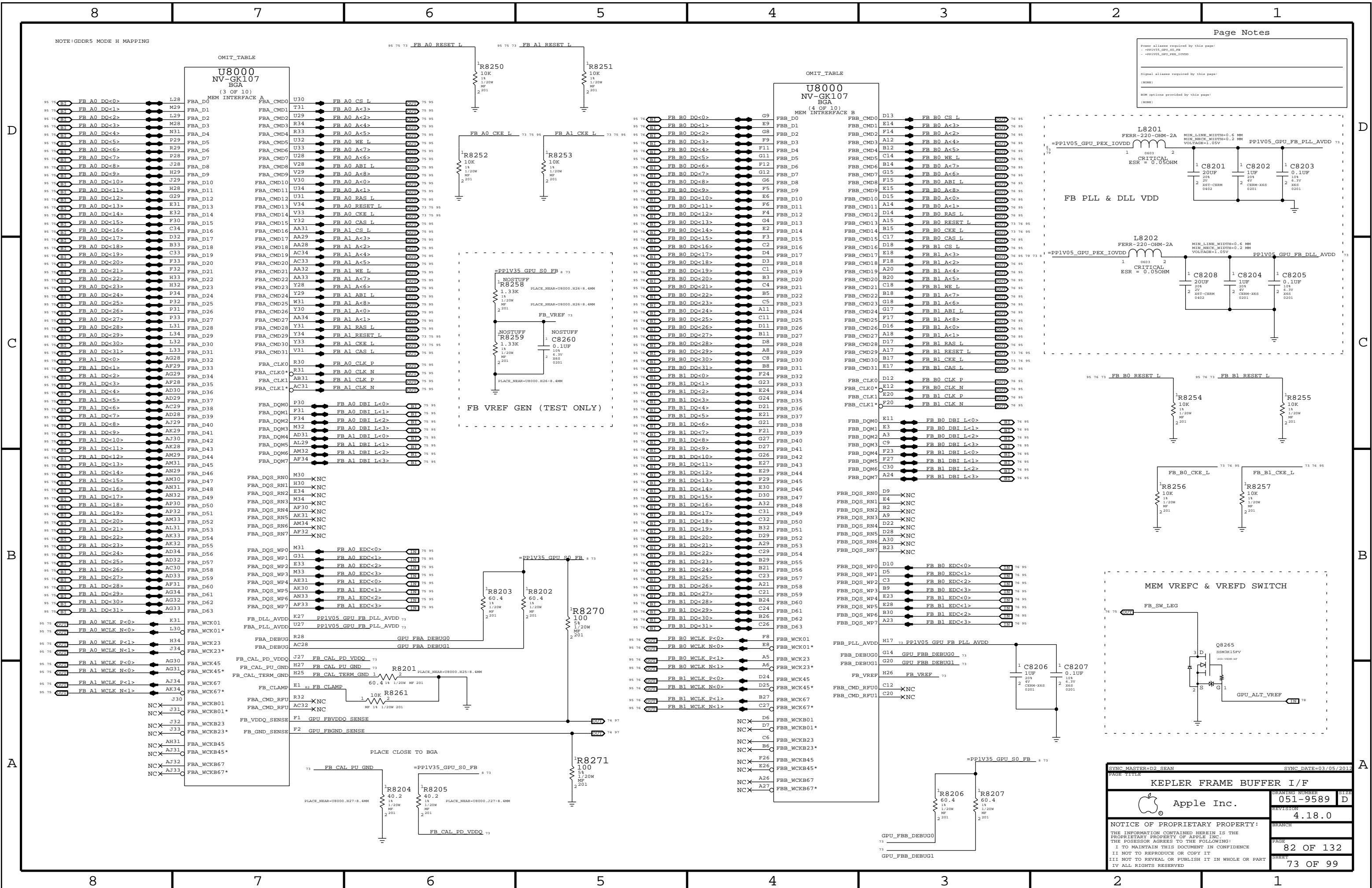
PAGE
79 OF 132

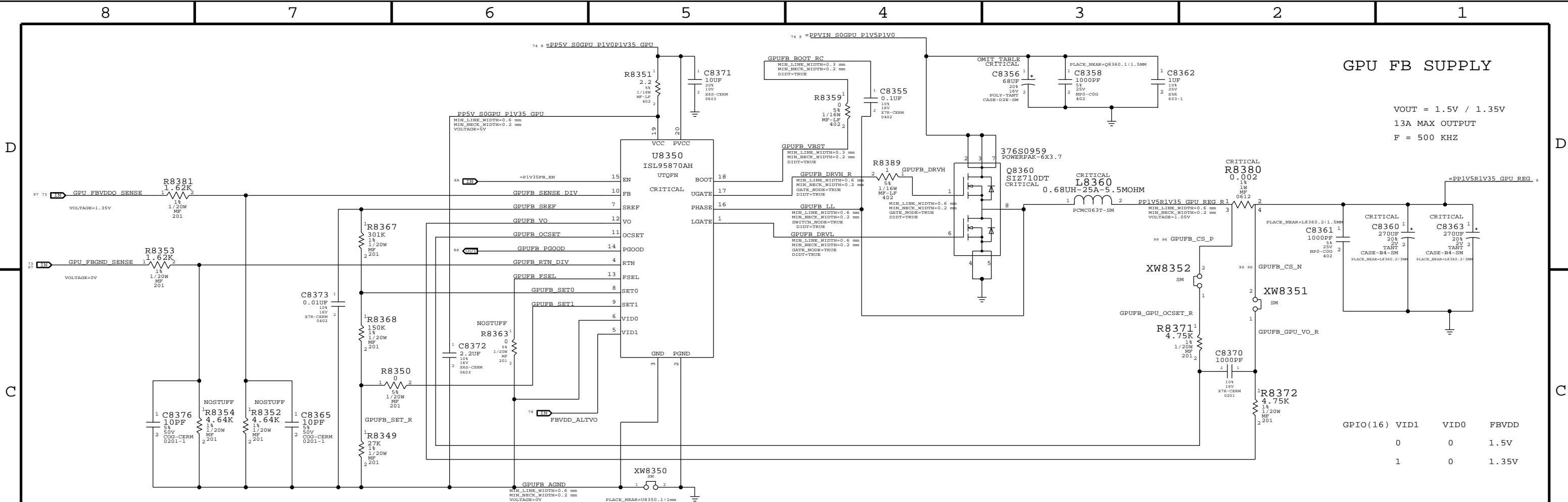
SHEET
70 OF 99



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
KEPLER PCI-E			
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		SHEET 71 OF 99	



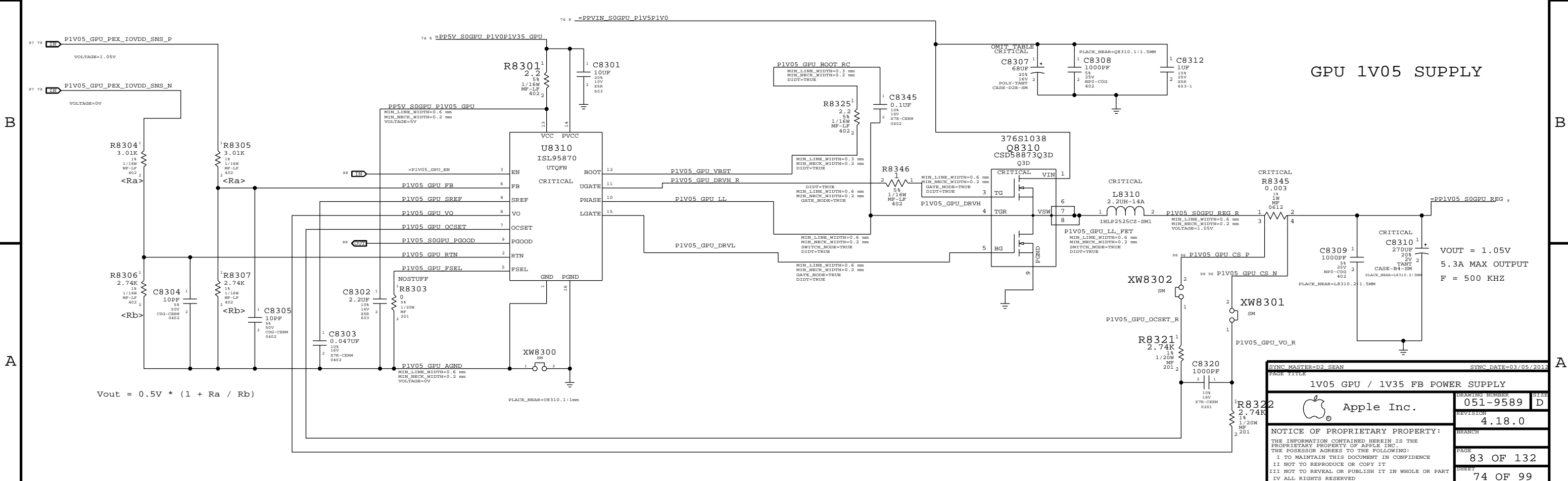




GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
0	0	1.5V	
1	0	1.35V	



GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

$V_{out} = 0.5V * (1 + R_a / R_b)$

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PAGE TITLE
1V05 GPU / 1V35 FB POWER SUPPLY

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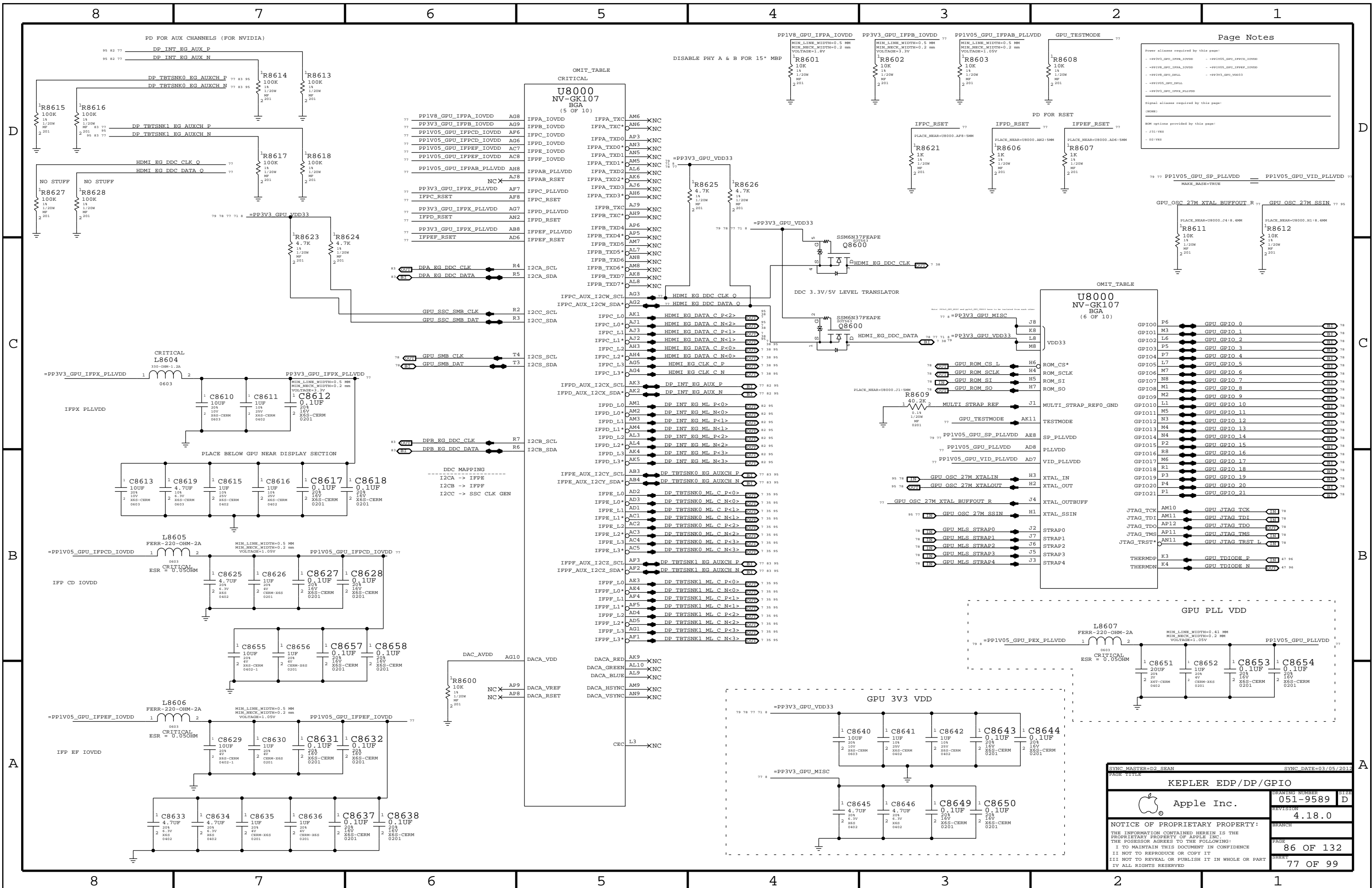
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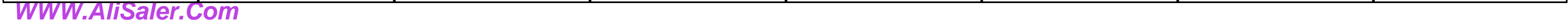
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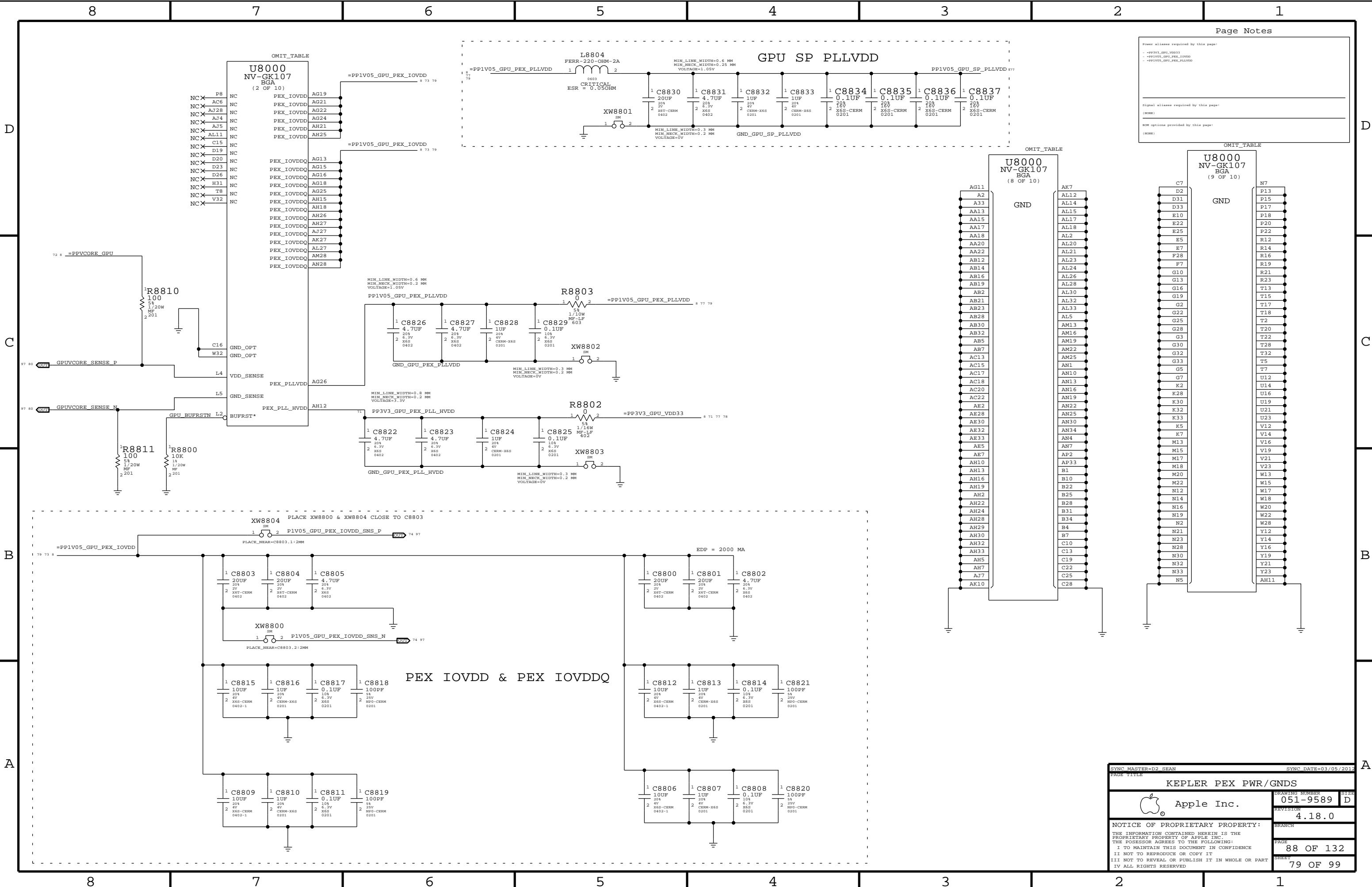
REVISION
4.18.0

PAGE
83 OF 132


SHEET
74 OF 99



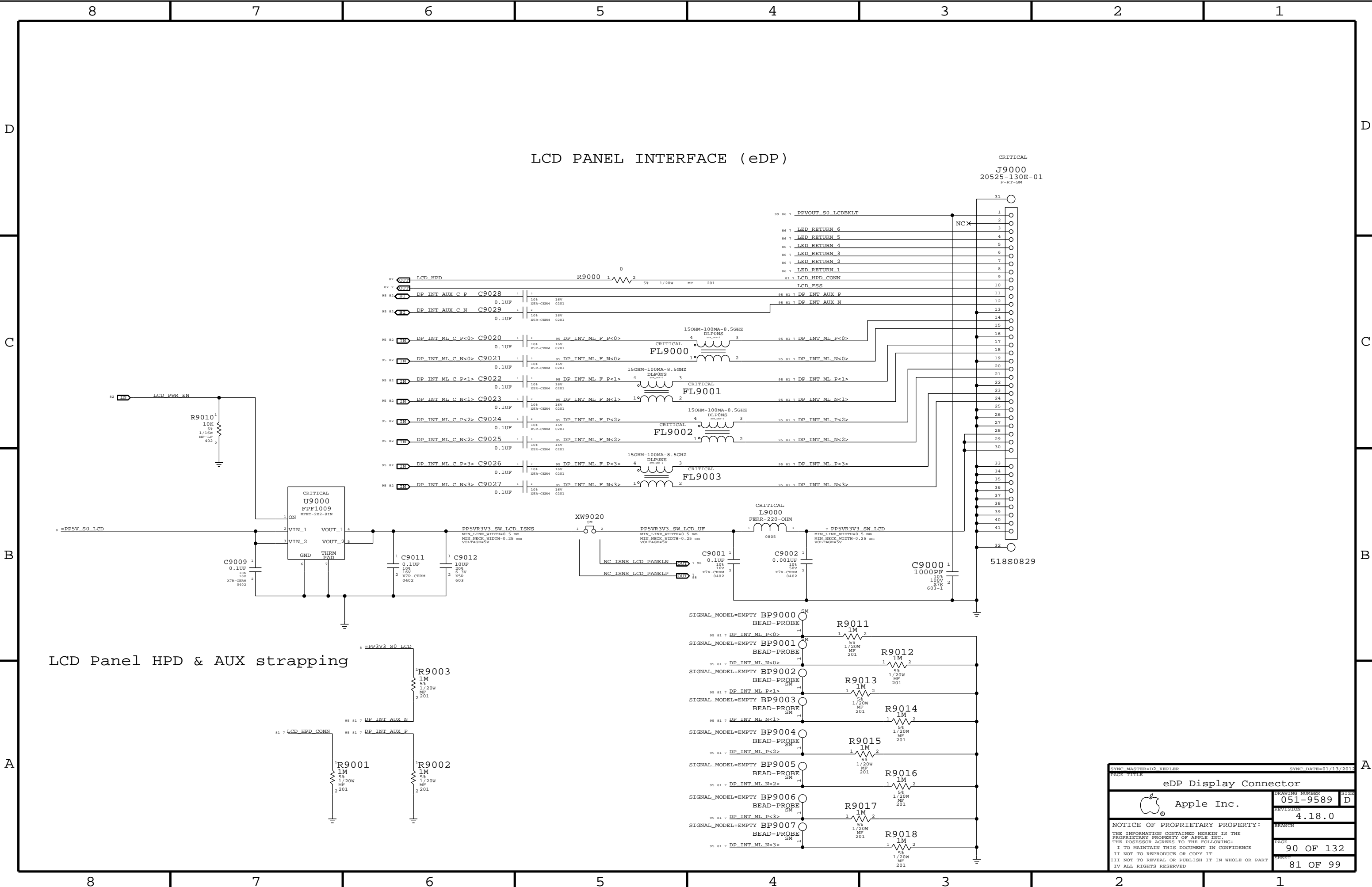





Page Notes	
Power aliases required by this page:	
- PP3V3_GPU_VDD33	
- PP1V05_GPU_PEX_IOVDD	
- PP1V05_GPU_PEX_PLLVDD	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

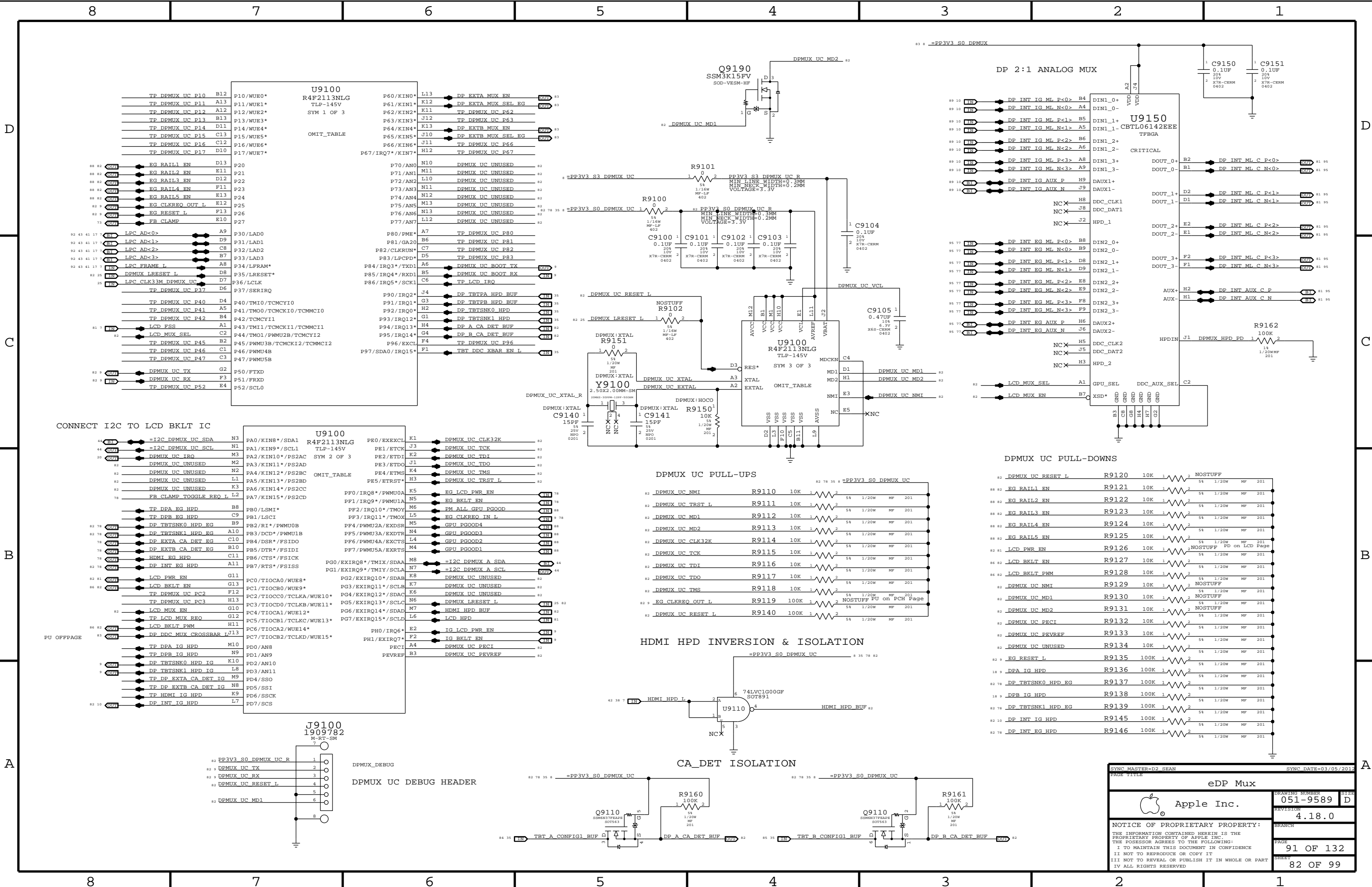
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PAGE TITLE			
KEPLER PEX PWR/GNDS			
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		PAGE	
		88 OF 132	
		SHEET	
		79 OF 99	





LCD Panel HPD & AUX strapping

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
eDP Display Connector			
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PAGE		90 OF 132	
SHEET		81 OF 99	




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PAGE TITLE

eDP Mux

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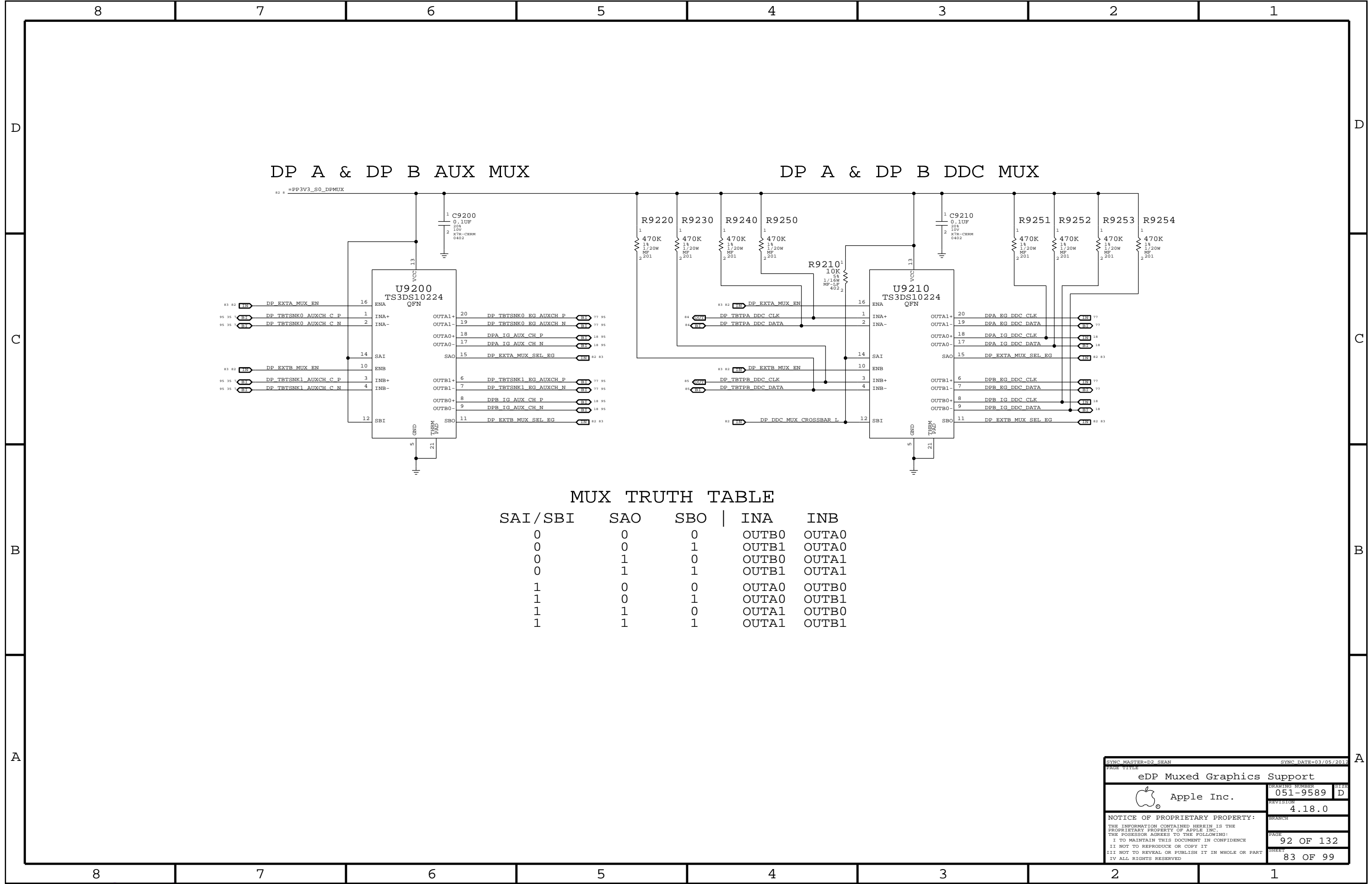
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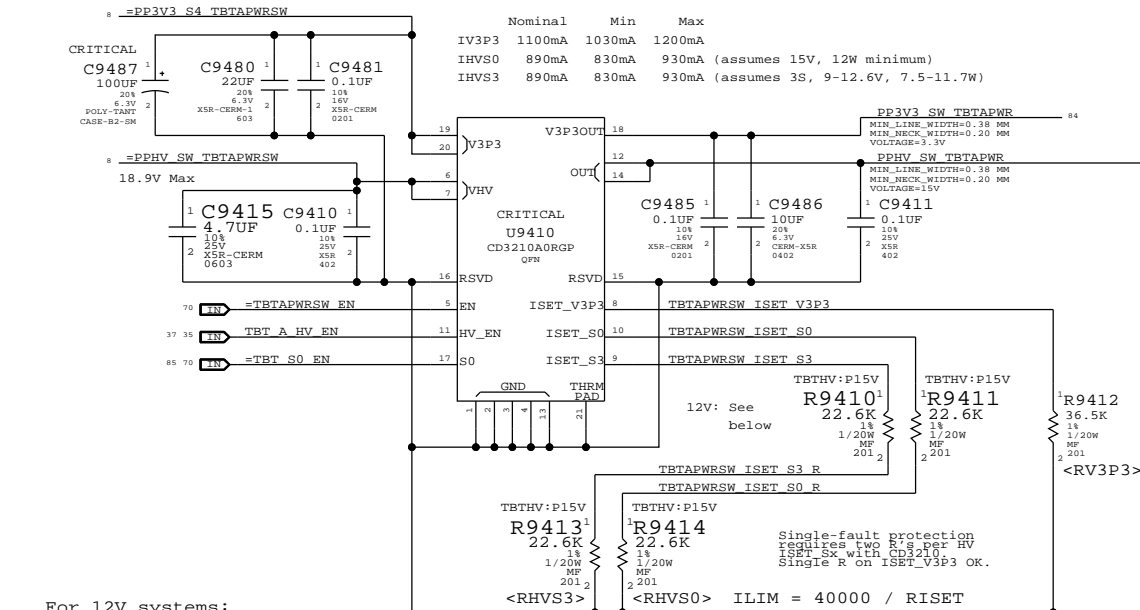
PAGE
91 OF 132

SHEET
82 OF 99

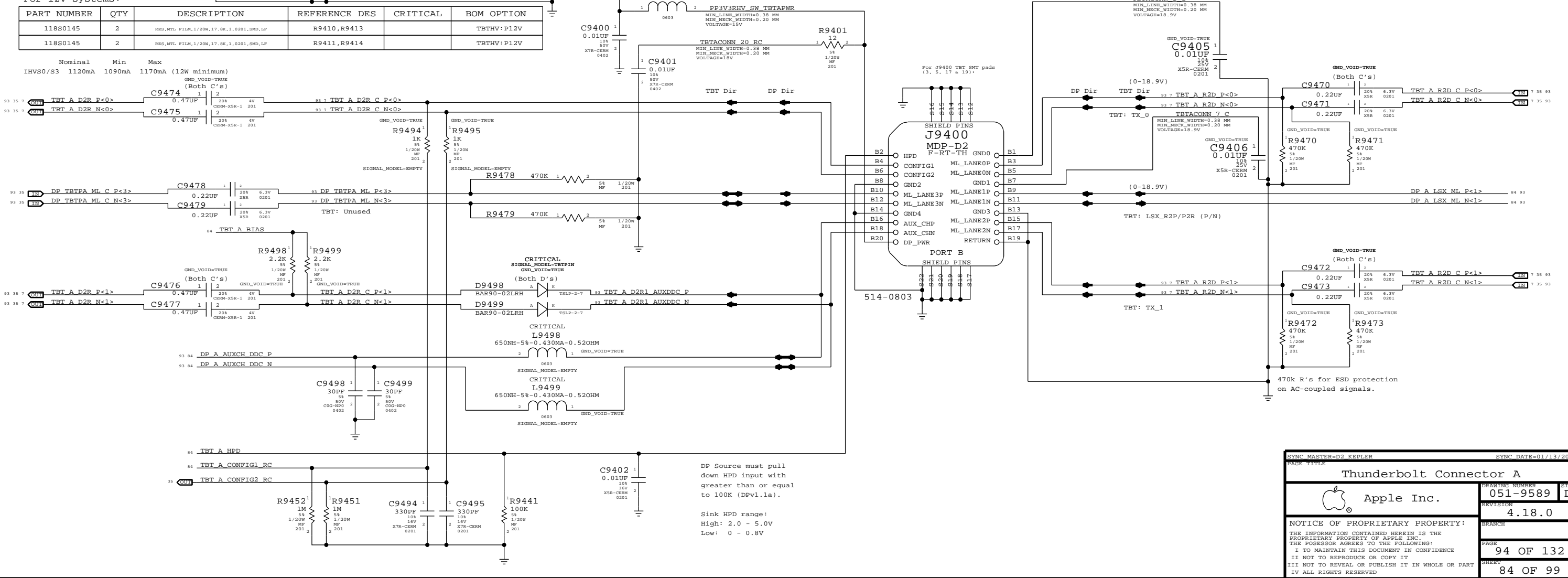


3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.



Thunderbolt Connector A



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Thunderbolt Connector A

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PAGE

94 OF 132

SHEET

84 OF 99

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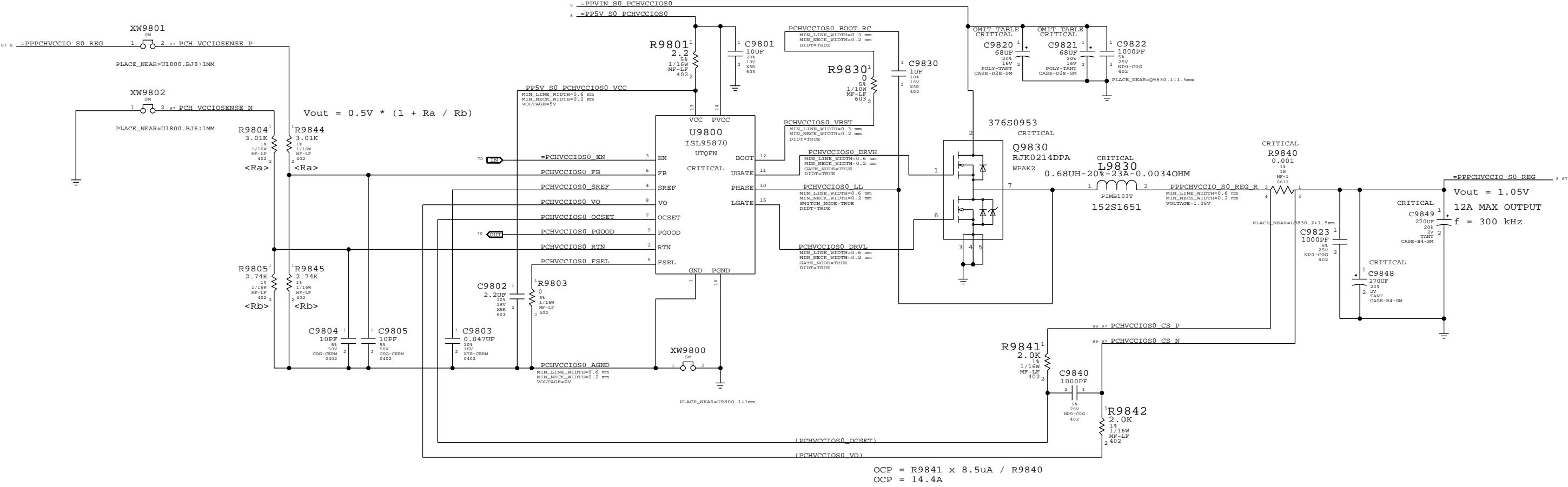
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PCH VCCIO (1.05V S0) REGULATOR



OCP = R9841 x 8.5uA / R9840
OCP = 14.4A

PCH VCCIO (1.05V) POWER SUPPLY	
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	PAGE 98 OF 132
	SHEET 87 OF 99

D

C

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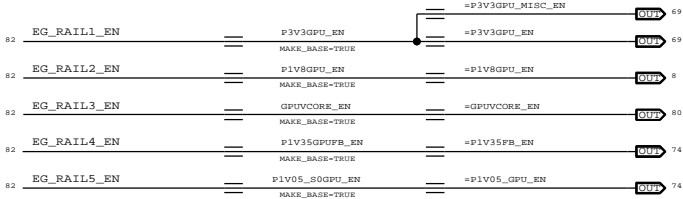
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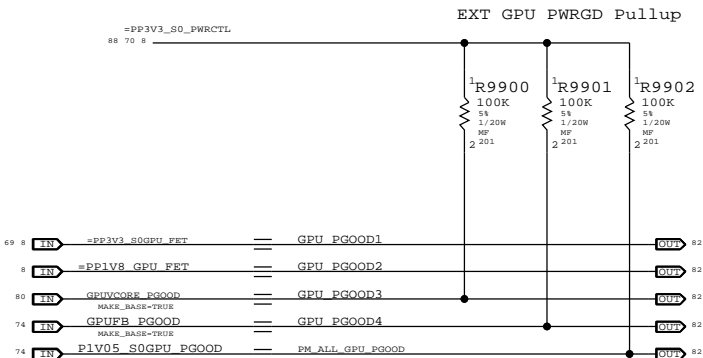
GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME UP in the following order:

- 1) GPU_3.3V
- 2) IFPX IOVDD - 1.8V
- 3) GPUVCORE
- 4) FBVDDQ/GDDR5 1.35V
- 5) PEKVDD/Q OR IFPY IOVDD - 1.05V



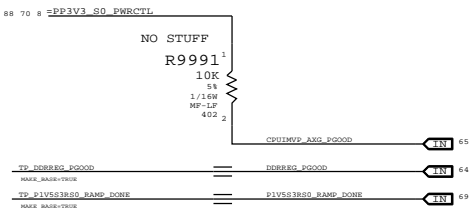
NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS



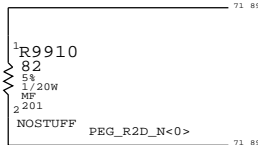
NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

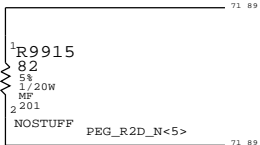
Unused PGOOD signal



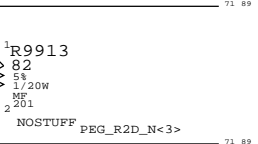
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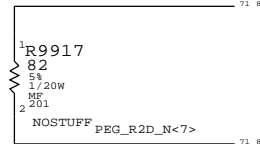
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PEG_R2D_P<3>



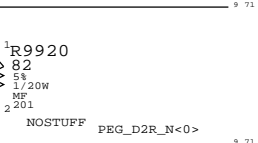
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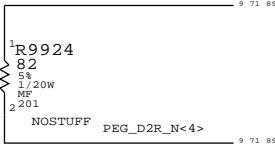
PLACE R9910 - R9917 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

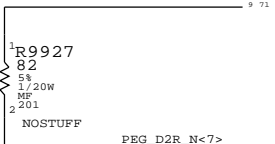
PEG_D2R_P<0>



PEG_D2R_P<4>



PEG_D2R_P<7>



PLACE R9920 - R9927 CLOSE TO U1000

8

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1

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Power Sequencing EG/PCH S0			
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8	7	6	5	4	3	2	1
CPU Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.							
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				
Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.							
SOURCE: IVB PLATFORM DG , Tables 205-207							
PCI-Express							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?	PCIE	TOP,BOTTOM	15 MIL	?
CLK_PCIE	*	20 MIL	?				
PEG							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
PEG_RXX	*	=4X_DIELECTRIC	?				
PEG_TXTX	*	=4X_DIELECTRIC	?				
PEG_TXRX	*	=10X_DIELECTRIC	?				
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET				
PEG_D2R	PEG_D2R	*	PEG_RXX				
PEG_R2D	PEG_R2D	*	PEG_TXTX				
PEG_D2R	PEG_R2D	*	PEG_TXRX				
CPU Net Properties							
ELECTRICAL_CONSTRAINT_SET				NET_TYPE			
		PHYSICAL	SPACING				
DMI_S2N	PCIE_85D	PCIE	DMI_S2N P<3:0>	10	18		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N N<3:0>	10	18		
DMI_N2S	PCIE_85D	PCIE	DMI_N2S P<3:0>	10	18		
DMI_N2S	PCIE_85D	PCIE	DMI_N2S N<3:0>	10	18		
FDI_DATA	PCIE_85D	PCIE	FDI_DATA P<7:0>	9	10		
FDI_DATA	PCIE_85D	PCIE	FDI_DATA N<7:0>	9	10		
FDI_FSYNC	CEU_50S	CEU_AGTL	FDI_FSYNC<1..0>	9	10		
FDI_FSYNC	CEU_50S	CEU_AGTL	FDI_FSYNC<1..0>	9	10		
FDI_INT	CEU_50S	CEU_AGTL	FDI_INT	10	18		
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU P	11	17		
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU N	11	17		
DP_INT_ML	DE_85D	DISPLAYPORT	DP_INT IG ML P<3:0>	10	82		
DP_INT_ML	DE_85D	DISPLAYPORT	DP_INT IG ML N<3:0>	10	82		
DP_INT_AUX	DE_85D	DISPLAYPORT	DP_INT IG AUX P	10	82		
DP_INT_AUX	DE_85D	DISPLAYPORT	DP_INT IG AUX N	10	82		
CPU_EDP_COMP	CEU_27P4S	CEU_COMP	CPU EDP COMP	10			
CPU_PEG_COMP	CEU_27P4S	CEU_COMP	CPU PEG COMP	10			
CPU_CFG	CEU_50S	CEU_ITP	CPU_CFG<17..0>	10	24		
VDR_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU CLK100M P	11	17		
VDR_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU CLK100M N	11	17		
XDP_CLK_BCH	CLK_PCIE_90D	CLK_PCIE	ITEXDP CLK100M P	17	24		
XDP_CLK_BCH	CLK_PCIE_90D	CLK_PCIE	ITEXDP CLK100M N	17	24		
DPLL_REF_CLKP	CLK_PCIE_90D	CLK_PCIE	DPLL_REF CLKP	9	11		
DPLL_REF_CLKN	CLK_PCIE_90D	CLK_PCIE	DPLL_REF CLKN	9	11		
XDP_CPU_TDI	CEU_50S	CEU_ITP	XDP CPU TDI	11	24		
VDR_TDI	CEU_50S	CEU_ITP	XDP CPU TDI	11	24		
XDP_TMS	CEU_50S	CEU_ITP	XDP CPU TMS	11	24		
XDP_TCK	CEU_50S	CEU_ITP	XDP CPU TCK	11	24		
VDR_TRST_L	CEU_50S	CEU_ITP	XDP CPU TRST L	11	24		
XDP_BPM	CEU_50S	CEU_ITP	XDP BPM L<3..0>	11	24		
XDP_BPM_L	CEU_50S	CEU_ITP	XDP BPM L<7..4>	11	24		
VDR_DBRESET_L	CEU_50S	CEU_ITP	XDP DBRESET L	11	24	25	
XDP_CPU_PRDY_L	CEU_50S	CEU_ITP	XDP CPU PRDY L	11	24		
XDP_CPU_PREQ_L	CEU_50S	CEU_ITP	XDP CPU PREQ L	11	24		
CPU_CATERR_L	CEU_50S	CEU_AGTL	CPU CATERR L	11	41		
CPU_PROC_SEL_L	CEU_50S	CEU_AGTL	CPU PROC_SEL L	11	20		
CPU_PECI	CEU_50S	CEU_VID	CPU Peci	11	20	42	
CPU_PROCHOT_L	CEU_50S	CEU_AGTL	CPU PROCHOT L	11	41	42	65
XDP_CPU_PWRGD	CEU_50S	CEU_ITP	XDP CPU PWRGD	24			
PM_THERMTRIP_L	CEU_50S	CEU_8MIL	PM_THERMTRIP L	11	20	42	
PM_SYNC	CEU_50S	CEU_AGTL	PM_SYNC	11	18		
PM_MEM_PWRGD	CEU_50S	CEU_AGTL	PM_MEM_PWRGD	11	18	27	
CPU_PWRGD	CEU_50S	CEU_AGTL	CPU_PWRGD	11	20	24	
CPU_SM_RCOMP	CEU_27P4S	CEU_COMP	CPU SM_RCOMP<2..0>	11			
CPU_VIDSOUT	CEU_VID	CEU_VID	CPU_VIDSOUT	13	65		
CPU_VIDALERT_L	CEU_VID	CEU_VID	CPU_VIDALERT L	13	65		
CPU_VIDSA_VID<1..0>	CEU_VID	CEU_VID	CPU_VIDSA_VID<1..0>	13	62		
CPU_VCCSENSE_P	CEU_27P4S	CEU_VCCSENSE	CPU_VCCSENSE_P	13	65		
CPU_VCCSENSE_N	CEU_27P4S	CEU_VCCSENSE	CPU_VCCSENSE_N	13	65		
CPU_VCCIOSENSE_P	CEU_27P4S	CEU_VCCIOSENSE	CPU_VCCIOSENSE_P	13	67		
CPU_VCCIOSENSE_N	CEU_27P4S	CEU_VCCIOSENSE	CPU_VCCIOSENSE_N	13	67		
CPU_AXG_SENSE_P	CEU_27P4S	CEU_VCCSENSE	CPU_AXG_SENSE_P	13	65		
CPU_AXG_SENSE_N	CEU_27P4S	CEU_VCCSENSE	CPU_AXG_SENSE_N	13	65		
CPU_VCC_VALSENSE_P	CEU_27P4S	CEU_VCCSENSE	CPU_VCC_VALSENSE_P	13			
CPU_VCC_VALSENSE_N	CEU_27P4S	CEU_VCCSENSE	CPU_VCC_VALSENSE_N	13			
CPU_AXG_VALSENSE_P	CEU_27P4S	CEU_VCCSENSE	CPU_AXG_VALSENSE_P	13			
CPU_AXG_VALSENSE_N	CEU_27P4S	CEU_VCCSENSE	CPU_AXG_VALSENSE_N	13			
CPU_VCCSASENSE	CEU_50S	CEU_AGTL	CPU_VCCSASENSE	13	62		
PPCPU_MEM_VREFDQ_A	CEU_VREF	CEU_VREF	PPCPU MEM_VREFDQ_A	10	33		
PPCPU_MEM_VREFDQ_B	CEU_VREF	CEU_VREF	PPCPU MEM_VREFDQ_B	10	33		
PP0V75_S3_MEM_VREFDQ_A	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFDQ_A	28	29	33	
PP0V75_S3_MEM_VREFDQ_B	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFDQ_B	30	31	33	
PP0V75_S3_MEM_VREFCA_A	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFCA_A	28	29	33	
PP0V75_S3_MEM_VREFCA_B	CEU_VREF	CEU_VREF	PP0V75_S3_MEM_VREFCA_B	30	31	33	
XDP_CPU_CLK100M_P	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M_P	24			
XDP_CPU_CLK100M_N	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M_N	24			
PEG_R2D P<7..0>	PEG_80D	PEG_R2D	PEG_R2D P<7..0>	71	88		
PEG_R2D N<7..0>	PEG_80D	PEG_R2D	PEG_R2D N<7..0>	71	88		
PEG_R2D C P<7..0>	PEG_80D	PEG_R2D	PEG_R2D C P<7..0>	9	71		
PEG_R2D C N<7..0>	PEG_80D	PEG_R2D	PEG_R2D C N<7..0>	9	71		
PEG_D2R P<7..0>	PEG_80D	PEG_D2R	PEG_D2R P<7..0>	9	71	88	
PEG_D2R N<7..0>	PEG_80D	PEG_D2R	PEG_D2R N<7..0>	9	71	88	
PEG_D2R C P<7..0>	PEG_80D	PEG_D2R	PEG_D2R C P<7..0>	71			
PEG_D2R C N<7..0>	PEG_80D	PEG_D2R	PEG_D2R C N<7..0>	71			
CPU Constraints							
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100 OF 132							
89 OF 99							

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	EDL1, EDL4, EDL6, EDL10	=4:1_SPACING	?	PCH_DISPLAYPORT	TOP, BOTTOM	=4:1_SPACING	?
LVDS	EDL1, EDL4, EDL6, EDL10	=4:1_SPACING	?	LVDS	TOP, BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	100, 100A, 100P, 100U	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA5	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	10L1, 10L4, 10L9, 10L10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	DBL3, LBL4, CRAP, LBL10	=5:1_SPACING	?	USB3	TOP, BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?


NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LVDS IG A CLK	LVDS_85d	LVDS	LVDS IG A CLK P 9 18
	LVDS IG A CLK	LVDS_85d	LVDS	LVDS IG A CLK N 9 18
	LVDS IG A DATA	LVDS_85d	LVDS	LVDS IG A DATA P<2..0> 9 18
	LVDS IG A DATA	LVDS_85d	LVDS	LVDS IG A DATA N<2..0> 9 18
	LVDS IG A DATA3	LVDS_85d	LVDS	LVDS IG A DATA P<3> 9 18
	LVDS IG A DATA3	LVDS_85d	LVDS	LVDS IG A DATA N<3> 9 18
	LVDS IG B DATA	LVDS_85d	LVDS	LVDS IG B DATA P<2..0> 9 18
	LVDS IG B DATA	LVDS_85d	LVDS	LVDS IG B DATA N<2..0> 9 18
	SATA HDD R2D	SATA_90d	SATA	SATA HDD R2D C P 17 39
	SATA HDD R2D	SATA_90d	SATA	SATA HDD R2D C N 17 39
	SATA HDD D2R	SATA_90d	SATA	SATA HDD D2R P 17 39
	SATA HDD D2R	SATA_90d	SATA	SATA HDD D2R N 17 39
	SATA HDD D2R	SATA_90d	SATA	SATA SSD D2R MUX OUT P 39
	SATA HDD D2R	SATA_90d	SATA	SATA SSD D2R MUX OUT N 39
	SATA HDD R2D	SATA_90d	SATA	SATA SSD R2D MUX IN P 39
	SATA HDD R2D	SATA_90d	SATA	SATA SSD R2D MUX IN N 39
938	SATA HDD D2R	SATA_90d	SATA	SATA SSD D2R P 39
939	SATA HDD R2D	SATA_90d	SATA	SATA SSD D2R N 39
940	SATA HDD R2D	SATA_90d	SATA	SATA SSD R2D P 39
941	SATA HDD R2D	SATA_90d	SATA	SATA SSD R2D N 39
942	SATA HDD R2D	SATA_90d	SATA	SATA HDD R2D UF P 39
943	SATA HDD R2D	SATA_90d	SATA	SATA HDD R2D UF N 39
	SATA ODD R2D	SATA_90d	SATA	SATA ODD R2D C P 9 17
	SATA ODD R2D	SATA_90d	SATA	SATA ODD R2D C N 9 17
	SATA ODD R2D	SATA_90d	SATA	SATA ODD R2D P 9 17
	SATA ODD R2D	SATA_90d	SATA	SATA ODD R2D N 9 17
	SATA ODD D2R	SATA_90d	SATA	SATA ODD D2R P 9 17
	SATA ODD D2R	SATA_90d	SATA	SATA ODD D2R N 9 17
	SATA ODD D2R	SATA_90d	SATA	SATA ODD D2R UF P 9 17
	SATA ODD D2R	SATA_90d	SATA	SATA ODD D2R UF N 9 17
944	ICH SATA3_1COMB	SATA_175d	SATA_1COMB	PCH SATA3COMP 17
945	ICH SATA_1COMB	SATA_175d	SATA_1COMB	PCH SATA1COMP 17
946	USB HUB1 UP	USB_85d	USB	USB EXTB XHCI P 19 26
947	USB HUB1 UP	USB_85d	USB	USB EXTB XHCI N 19 26
948	USB HUB1 UP	USB_85d	USB	USB EXTB EHCI P 19 26
949	USB HUB1 UP	USB_85d	USB	USB EXTB EHCI N 19 26
950	USB HUB2 UP	USB_85d	USB	USB HUB UP P 19 26
951	USB HUB2 UP	USB_85d	USB	USB HUB UP N 19 26
952	USB EXTA	USB_85d	USB	USB EXTA P 19 40
953	USB EXTB	USB_85d	USB	USB EXTB N 19 40
954	USB EXTB	USB_85d	USB	USB EXTB P 7 26 38
955	USB EXTB	USB_85d	USB	USB EXTB N 7 26 38
956	USB EXTC	USB_85d	USB	USB EXTC P 9 19
957	USB EXTC	USB_85d	USB	USB EXTC N 9 19
958	USB CAMERA	USB_85d	USB	USB CAMERA CONN P 7 34
959	USB BT	USB_85d	USB	USB CAMERA CONN N 7 34
960	USB BT	USB_85d	USB	USB BT P 9 34
961	USB BT	USB_85d	USB	USB BT CONN P 7 34
962	USB BT	USB_85d	USB	USB BT CONN N 7 34
963	USB BT	USB_85d	USB	USB BT WAKE P 34
964	USB BT	USB_85d	USB	USB BT WAKE N 34
965	USB TPAD	USB_85d	USB	USB TPAD P 9 49
966	USB TPAD	USB_85d	USB	USB TPAD N 9 49
967	USB IR	USB_85d	USB	USB SMC P 9 41
968	USB IR	USB_85d	USB	USB SMC N 9 41
969	ICH USB WB1AS	ICH_USB_WB1AS	ICH_USB1AS	PCH USB RB1AS 19
970	USB F23A	USB_85d	USB	USB EXTD XHCI P 19 26
971	USB F23A	USB_85d	USB	USB EXTD XHCI N 19 26
972	USB EXTA	USB_85d	USB	USB EXTA MIXED P 40
973	USB EXTA	USB_85d	USB	USB EXTA MIXED N 40
974	USB CAMERA	USB_85d	USB	USB CAMERA P 19 34
975	USB CAMERA	USB_85d	USB	USB CAMERA N 19 34
976	USB EXTA	USB_85d	USB	USB LTI P 40
977	USB EXTA	USB_85d	USB	USB LTI N 40
978	USB3 EXTB_TX	USB_85d	USB3	USB3 EXTB TX P 19 38
979	USB3 EXTB_TX	USB_85d	USB3	USB3 EXTB TX N 19 38
980	USB3 EXTB_RX	USB_85d	USB3	USB3 EXTB RX P 7 19 38
981	USB3 EXTB_RX	USB_85d	USB3	USB3 EXTB RX N 7 19 38
982	USB3 EXTC_TX	USB_85d	USB3	USB3 EXTC TX P 9 19
983	USB3 EXTC_TX	USB_85d	USB3	USB3 EXTC TX N 9 19
984	USB3 EXTC_RX	USB_85d	USB3	USB3 EXTC RX P 9 19
985	USB3 EXTC_RX	USB_85d	USB3	USB3 EXTC RX N 9 19
986	USB3 EXTA_TX	USB_85d	USB3	USB3 EXTA TX P 19 40
987	USB3 EXTA_TX	USB_85d	USB3	USB3 EXTA TX N 19 40
988	USB3 EXTA_RX	USB_85d	USB3	USB3 EXTA RX P 19 40
989	USB3 EXTA_RX	USB_85d	USB3	USB3 EXTA RX N 19 40

Clock Net Properties

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
RTN	SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC 17 26
RTN	SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 17 25
RTN		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB R 17
RTN	SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET 17
RTN		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET R
RTN	SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT 26 35
RTN		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT R 35

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		PAGE 102 OF 132	
		SHEET 91 OF 99	

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET			NET_TYPE		
PHYSICAL			SPACING		
	LPC_AD	LPC 508	LPC	LPC_AD<3...0>	7 17 41 43 82
	LPC_FRAME_L	LPC 508	LPC	LPC_FRAME_L	7 17 41 43 82
	LPC_RESET_L	LPC 508	LPC	LPC_RESET_L	25
	PCIE_CLK_LPC0	CLK LPC 508	CLK LPC	LPC_CLK33M_SMC_R	19 25
		CLK LPC 508	CLK LPC	LPC_CLK33M_SMC	25 41
		CLK LPC 508	CLK LPC	LPC_CLK33M_LPCPLUS	7 25 43
	SMBUS_PCH_CLK	SMR 508	SMR	SMBUS_PCH_CLK	17 44
	SMBUS_PCH_DATA	SMR 508	SMR	SMBUS_PCH_DATA	17 44
	SMBUS_PCH_0_CLK	SMR 508	SMR	SML_PCH_0_CLK	17 44
	SMBUS_PCH_0_DATA	SMR 508	SMR	SML_PCH_0_DATA	17 44
	SMBUS_PCH_1_CLK	SMR 508	SMR	SML_PCH_1_CLK	17 44
	SMBUS_PCH_1_DATA	SMR 508	SMR	SML_PCH_1_DATA	17 44
	HDA_RST_CLK	HDA 508	HDA	HDA_BIT_CLK	17 53
		HDA 508	HDA	HDA_BIT_CLK_R	17
	HDA_SYNC	HDA 508	HDA	HDA_SYNC	17 53
		HDA 508	HDA	HDA_SYNC_R	17
	HDA_RST_L	HDA 508	HDA	HDA_RST_R_L	17
		HDA 508	HDA	HDA_RST_L	17 53
	HDA_SDIO0	HDA 508	HDA	HDA_SDIO0	17 53
		HDA 508	HDA	AUD_SDI_R	53
	HDA_SDOUIT	HDA 508	HDA	HDA_SDOUIT	17 53
		HDA 508	HDA	HDA_SDOUIT_R	17 25
	SPT_CLK	SPT 558	SPT	SPI_CLK_R	17 43
		SPT 558	SPT	SPI_CLK	43
	SPT_MOSI	SPT 558	SPT	SPI_MOSI_R	17 43
		SPT 558	SPT	SPI_MOSI	43
	SPT_MISO	SPT 558	SPT	SPI_MISO	17 43
	SPT_CS0	SPT 558	SPT	SPI_CS0_R_L	17 43
		SPT 558	SPT	SPI_CS0_L	43
	PCIE_ENET_R2D	PCIE 85D	PCIE	PCIE_ENET_R2D_P	
		PCIE 85D	PCIE	PCIE_ENET_R2D_N	
	PCIE_ENET_R2D	PCIE 85D	PCIE	PCIE_ENET_R2D_C_P	7 17 38
		PCIE 85D	PCIE	PCIE_ENET_R2D_C_N	7 17 38
	PCIE_ENET_D2R	PCIE 85D	PCIE	PCIE_ENET_D2R_P	7 17 38
		PCIE 85D	PCIE	PCIE_ENET_D2R_N	7 17 38
		PCIE 85D	PCIE	PCIE_ENET_D2R_C_P	
		PCIE 85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_AP_R2D	PCIE 85D	PCIE	PCIE_AP_R2D_P	7 34
		PCIE 85D	PCIE	PCIE_AP_R2D_N	7 34
	PCIE_AP_R2D	PCIE 85D	PCIE	PCIE_AP_R2D_C_P	17 34
		PCIE 85D	PCIE	PCIE_AP_R2D_C_N	17 34
	PCIE_AP_D2R	PCIE 85D	PCIE	PCIE_AP_D2R_P	17 34
		PCIE 85D	PCIE	PCIE_AP_D2R_N	17 34
197D	PCIE_AP_D2R	PCIE 85D	PCIE	PCIE_AP_D2R_PI_P	7 34
198D		PCIE 85D	PCIE	PCIE_AP_D2R_PI_N	7 34
197D	PCIE_AP_D2R	PCIE 85D	PCIE	PCIE_AP_R2D_PI_P	34
198D		PCIE 85D	PCIE	PCIE_AP_R2D_PI_N	34
	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE SSD D2R MUX OUT_P	39
		PCIE 85D	PCIE	PCIE SSD D2R MUX OUT_N	39
	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE SSD R2D_C P<1...0>	9 39
		PCIE 85D	PCIE	PCIE SSD R2D_C N<1...0>	9 39
	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE SSD D2R P<1...0>	9 39
		PCIE 85D	PCIE	PCIE SSD D2R N<1...0>	9 39
	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE SSD R2D MUX IN_P	39
		PCIE 85D	PCIE	PCIE SSD R2D MUX IN_N	39
198D	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE SSD D2R_C P<1>	39
198D		PCIE 85D	PCIE	PCIE SSD D2R_C N<1>	39
198D	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE SSD R2D P<1>	39
198D		PCIE 85D	PCIE	PCIE SSD R2D N<1>	39
197D	PCIE_CLK100M	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_PCH_P	17
198D		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_PCH_N	17
197D	PCIE_CLK100M_TBT	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_TBT_P	17 35
198D		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_TBT_N	17 35
197D		CLK_PCIE 50D	CLK_PCIE	PCH_CLK96M_DOT_P	17
198D		CLK_PCIE 50D	CLK_PCIE	PCH_CLK96M_DOT_N	17
198D	PCIE_CLK100M_TBT	CLK_PCIE 50D	CLK_PCIE	PCH_CLK100M_SATA_P	17
198D		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_SATA_N	17
197D		CLK_508	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
198D		CLK_508	CLK_PCIE	LPC_CLK33M_PCIN	17 25
198D	PCIE_CLK100M	1:1 DIFFERENTIAL	CLK_PCIE	PEX_TSTCLK_O_P	71 95
197D		1:1 DIFFERENTIAL	CLK_PCIE	PEX_TSTCLK_O_N	71 95
	PCIE_CLK100M	CLK_PCIE 50D	CLK_PCIE	PEG_CLK100M_P	17 71
		CLK_PCIE 50D	CLK_PCIE	PEG_CLK100M_N	17 71
	PCIE_CLK100M_ENET	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 38
		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 38
	PCIE_CLK100M_AP	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_AP_P	17 34
		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_AP_N	17 34
	PCIE_CLK100M_FW	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_FW_P	9 17
		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_FW_N	9 17
198D	PCIE_CLK100M_FW	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_SSD_P	17 39
197D		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_SSD_N	17 39
198D	PCIE_CLK100M_EXCARD	CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
197D		CLK_PCIE 50D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE_TBT_R2D_C P<3...0>	9 35
198D	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE_TBT_R2D_C N<3...0>	9 35
197D	PCIE_TBT_R2D	PCIE 85D	PCIE	PCIE_TBT_R2D_P<3...0>	35
198D		PCIE 85D	PCIE	PCIE_TBT_R2D N<3...0>	35
197D	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE_TBT_D2R_P<3...0>	9 35
198D	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE_TBT_D2R N<3...0>	9 35
197D	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE_TBT_D2R_C P<3...0>	35
198D	PCIE_TBT_D2R	PCIE 85D	PCIE	PCIE_TBT_D2R_C N<3...0>	35

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
PCH Constraints 2			
	Apple Inc.		DRAWING NUMBER 051-9589
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		BRANCH 	PAGE 103 OF 132
		SHEET 92 OF 99	



8

7

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SMC Constraints

Apple Inc.

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051-9589

REVISION

4.18.0

BRANCH

PAGE

106 OF 132

SHEET

94 OF 99

SIZE

D

SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

8

7

6

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?	GDDR5_CLK	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?	GDDR5_CMD	TOP, BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?	GDDR5_DATA	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?	GDDR5_EDC	TOP, BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.

DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.

MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SIGNAL	
FEIN	FB_A0_CLK	gddr5_80n	gddr5_clk	FB A0 CLK P
FEIN	FB_A0_CLK	gddr5_80n	gddr5_clk	FB A0 CLK N
FEIN	FB_A1_CLK	gddr5_80n	gddr5_clk	FB A1 CLK P
FEIN	FB_A1_CLK	gddr5_80n	gddr5_clk	FB A1 CLK N
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 A<8...0>
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 A<8...0>
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 ABI L
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 ABI L
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 RAS L
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 RAS L
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 CAS L
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 CAS L
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 WE L
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 WE L
FEIN	FB_A0_CMD_R	gddr5_455se	gddr5_cmd	FB A0 CKE L
FEIN	FB_A1_CMD_R	gddr5_455se	gddr5_cmd	FB A1 CKE L
FEIN	FB_A0_CMD	gddr5_455se	gddr5_cmd	FB A0 CS L
FEIN	FB_A1_CMD	gddr5_455se	gddr5_cmd	FB A1 CS L
FEIN	FB_A0_EDC0	gddr5_455se	gddr5_edc	FB A0 EDC<0>
FEIN	FB_A0_EDC1	gddr5_455se	gddr5_edc	FB A0 EDC<1>
FEIN	FB_A0_EDC2	gddr5_455se	gddr5_edc	FB A0 EDC<2>
FEIN	FB_A0_EDC3	gddr5_455se	gddr5_edc	FB A0 EDC<3>
FEIN	FB_A1_EDC0	gddr5_455se	gddr5_edc	FB A1 EDC<0>
FEIN	FB_A1_EDC1	gddr5_455se	gddr5_edc	FB A1 EDC<1>
FEIN	FB_A1_EDC2	gddr5_455se	gddr5_edc	FB A1 EDC<2>
FEIN	FB_A1_EDC3	gddr5_455se	gddr5_edc	FB A1 EDC<3>
FEIN	FB_A0_DBI_L0	gddr5_455se	gddr5_data	FB A0 DBI L<0>
FEIN	FB_A0_DBI_L1	gddr5_455se	gddr5_data	FB A0 DBI L<1>
FEIN	FB_A0_DBI_L2	gddr5_455se	gddr5_data	FB A0 DBI L<2>
FEIN	FB_A0_DBI_L3	gddr5_455se	gddr5_data	FB A0 DBI L<3>
FEIN	FB_A1_DBI_L0	gddr5_455se	gddr5_data	FB A1 DBI L<0>
FEIN	FB_A1_DBI_L1	gddr5_455se	gddr5_data	FB A1 DBI L<1>
FEIN	FB_A1_DBI_L2	gddr5_455se	gddr5_data	FB A1 DBI L<2>
FEIN	FB_A1_DBI_L3	gddr5_455se	gddr5_data	FB A1 DBI L<3>
FEIN	FB_A0_WCLK0	gddr5_80n	gddr5_cmd	FB A0 WCLK P<0>
FEIN	FB_A0_WCLK0	gddr5_80n	gddr5_cmd	FB A0 WCLK N<0>
FEIN	FB_A0_WCLK1	gddr5_80n	gddr5_cmd	FB A0 WCLK P<1>
FEIN	FB_A0_WCLK1	gddr5_80n	gddr5_cmd	FB A0 WCLK N<1>
FEIN	FB_A1_WCLK0	gddr5_80n	gddr5_cmd	FB A1 WCLK P<0>
FEIN	FB_A1_WCLK0	gddr5_80n	gddr5_cmd	FB A1 WCLK N<0>
FEIN	FB_A1_WCLK1	gddr5_80n	gddr5_cmd	FB A1 WCLK P<1>
FEIN	FB_A1_WCLK1	gddr5_80n	gddr5_cmd	FB A1 WCLK N<1>
FEIN	FB_A0_DQ_BYTE0	gddr5_455se	gddr5_data	FB A0 DQ<7...0>
FEIN	FB_A0_DQ_BYTE1	gddr5_455se	gddr5_data	FB A0 DQ<15...8>
FEIN	FB_A0_DQ_BYTE2	gddr5_455se	gddr5_data	FB A0 DQ<23...16>
FEIN	FB_A0_DQ_BYTE3	gddr5_455se	gddr5_data	FB A0 DQ<31...24>
FEIN	FB_A1_DQ_BYTE0	gddr5_455se	gddr5_data	FB A1 DQ<7...0>
FEIN	FB_A1_DQ_BYTE1	gddr5_455se	gddr5_data	FB A1 DQ<15...8>
FEIN	FB_A1_DQ_BYTE2	gddr5_455se	gddr5_data	FB A1 DQ<23...16>
FEIN	FB_A1_DQ_BYTE3	gddr5_455se	gddr5_data	FB A1 DQ<31...24>
FEIN	FB_A0_CMD_R	gddr5_455se	gddr5_cmd	FB A0 RESET L
FEIN	FB_A1_CMD_R	gddr5_455se	gddr5_cmd	FB A1 RESET L

GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		SYMBOL	STRING	
PARAM	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P
PARAM	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N
PARAM	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P
PARAM	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 A<8...0>
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 A<8...0>
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 ABI L
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 ABI L
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 RAS L
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 RAS L
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CAS L
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CAS L
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 WE L
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 WE L
PARAM	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 CKE L
PARAM	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 CKE L
PARAM	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CS L
PARAM	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CS L
PARAM	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>
PARAM	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>
PARAM	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>
PARAM	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>
PARAM	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>
PARAM	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>
PARAM	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>
PARAM	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>
PARAM	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>
PARAM	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>
PARAM	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>
PARAM	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>
PARAM	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>
PARAM	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>
PARAM	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>
PARAM	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>
PARAM	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>
PARAM	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>
PARAM	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>
PARAM	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>
PARAM	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>
PARAM	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>
PARAM	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>
PARAM	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>
PARAM	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7...0>
PARAM	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15...8>
PARAM	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23...16>
PARAM	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31...24>
PARAM	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7...0>
PARAM	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15...8>
PARAM	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23...16>
PARAM	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31...24>
PARAM	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 RESET L
PARAM	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 RESET L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		FEED	END
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML C P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP INT ML C N<3..0>
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT AUX C P
DP_85N	DP_85N	DISPLAYPORT	DP INT AUX C N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT AUX P
DP_85N	DP_85N	DISPLAYPORT	DP INT AUX N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT EG AUX P
DP_85N	DP_85N	DISPLAYPORT	DP INT EG AUX N
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP INT ML N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP INT ML F N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT EG ML P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP INT EG ML N<3..0>
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPA IG AUX CH P
DP_85N	DP_85N	DISPLAYPORT	DPA IG AUX CH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPB IG AUX CH P
DP_85N	DP_85N	DISPLAYPORT	DPB IG AUX CH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSN0 EG AUXCH P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN0 EG AUXCH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSN1 EG AUXCH P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN1 EG AUXCH N
TBT_A_AUXCH	DP_85N	DISPLAYPORT	DP TBSN0 AUXCH C P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN0 AUXCH C N
TBT_B_AUXCH	DP_85N	DISPLAYPORT	DP TBSN1 AUXCH C P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN1 AUXCH C N
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSN0 ML C P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP TBSN0 ML C N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSN1 ML C P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP TBSN1 ML C N<3..0>
TBT_A_AUXCH	DP_85N	DISPLAYPORT	DP TBSN0 AUXCH P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN0 AUXCH N
TBT_B_AUXCH	DP_85N	DISPLAYPORT	DP TBSN1 AUXCH P
DP_85N	DP_85N	DISPLAYPORT	DP TBSN1 AUXCH N
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSN0 ML P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP TBSN0 ML N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSN1 ML P<3..0>
DP_85N	DP_85N	DISPLAYPORT	DP TBSN1 ML N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET		PROPERTY	DEF_TYPE	AFFECTED	
	GPU_CLK27M	CLK_STOP_55C	CLK_STOP	GPU_OSC_27M_XTALIN	77 78
	GPU_CLK27M	CLK_STOP_55C	CLK_STOP	GPU_OSC_27M_XTALOUT	77 78
	GPU_CLK27M	CLK_STOP_55C	CLK_STOP	GPU_OSC_27M_XTAL_BUFFOUT	
	GPU_CLK27M	CLK_STOP_55C	CLK_STOP	GPU_OSC_27M_SSIN	77
		1:1_DIEFPAIR		PEX_TSTCLK_O_P	71 92
		1:1_DIEFPAIR		PEX_TSTCLK_O_N	71 92
	HDMI_DATA	HDMI_50D	HDMI	HDMI_EG_DATA_C_P<2..0>	7 38
		HDMI_50D	HDMI	HDMI_EG_DATA_C_N<2..0>	7 38
	HDMI_CLK	HDMI_50D	HDMI	HDMI_EG_CLK_C_P	7 38
		HDMI_50D	HDMI	HDMI_EG_CLK_C_N	7 38

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
GPU (Kepler) CONSTRAINTS			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9589		D
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		107 OF 132	
		SHEET	
		95 OF 99	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_550	*	>1:1_DIFFPAIR	>55_OHM_SE	>55_OHM_SE	>55_OHM_SE	>1:1_DIFFPAIR	>1:1_DIFFPAIR
THERM_I701_550	*	>1:1_DIFFPAIR	>55_OHM_SE	>55_OHM_SE	>55_OHM_SE	>1:1_DIFFPAIR	>1:1_DIFFPAIR
DIFFPAIR	*	>1:1_DIFFPAIR			>1:1_DIFFPAIR	>1:1_DIFFPAIR	>1:1_DIFFPAIR
AIRIODIFF	*	>1:1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.3 MM	0.3 MM
THERM_550_C01UMW01NS01	*	>1:1_DIFFPAIR	>55_OHM_SE	>55_OHM_SE	>55_OHM_SE	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	-2:1_SPACING	?
THERM	*	-2:1_SPACING	?
AUDIO	*	-2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VOCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	-STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2000 <small>net_type: GND, spacing_rule: P2000</small>
PCIE	GND	*	GND_P2000 <small>net_type: GND, spacing_rule: P2000</small>
SATA	GND	*	GND_P2000 <small>net_type: GND, spacing_rule: P2000</small>
USB	GND	*	GND_P2000 <small>net_type: GND, spacing_rule: P2000</small>
CLK_PCIE	SR_POWER	*	PWR_P2000 <small>net_type: SR_POWER, spacing_rule: P2000</small>
SATA	SR_POWER	*	PWR_P2000 <small>net_type: SR_POWER, spacing_rule: P2000</small>
USB	SR_POWER	*	PWR_P2000 <small>net_type: SR_POWER, spacing_rule: P2000</small>

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P200M	*	0.20 MM	1000
PWR_P200M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2004
GND	MEM_CMD	*	GND_P2004
GND	MEM_CTL	*	GND_P2004
GND	MEM_*_DQ_BITE*	*	GND_P2004
GND	MEM_DQS	*	GND_P2004

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_8SD	BGA	LVDS_8SD
DP_8SD	BGA	100_DIFF_BGA
SATA_9SD	BGA	100_DIFF_BGA
CLK_PCIE_9SD	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		CIN
		PHYSICAL		
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUTIMENS D2 P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUTIMENS D2 N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	DDR3TIMENS D1 P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	DDR3TIMENS D1 N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUTIMENS D P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUTIMENS D N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPU_TDIODE P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPU_TDIODE N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	VCCSA0 CS_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	VCCSA0 CS_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	VCCRA1SENSE R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	VCCRA1SENSE R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LV5 MEM R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LV5 MEM R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUVCCIO0 CS_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUVCCIO0 CS_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUVCCIO1SENSE R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUVCCIO1SENSE R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUISENSE_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUISENSE_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LV5 MEM_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LV5 MEM_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS AIRPORT_R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LCDCLKIT_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS LCDCLKIT_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUPB_CS_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	GPUPB_CS_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V0_S0GPU_R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V0_S0GPU_R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V8_S0GPU_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V8_S0GPU_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V8_S0GPU_R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V8_S0GPU_R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	P1V05_GPU_CS_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	P1V05_GPU_CS_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V5_S0GPU_R_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS PP1V5_S0GPU_R_N
	GROUP_DIFFPAIR1_#1	GROUP1001_55G	GROUP1001	CPUIMVP_ISNSIG_P
	GROUP_DIFFPAIR1_#2	GROUP1001_55G	GROUP1001	CPUIMVP_ISNSIG_N
	GROUP_DIFFPAIR1_#3	GROUP1001_55G	GROUP1001	CPUIMVP_ISNSIG_R_P
	GROUP_DIFFPAIR1_#4	GROUP1001_55G	GROUP1001	CPUIMVP_ISNSIG_R_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_OTHER_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_OTHER_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_GPU_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_GPU_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_COMPUTING_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	ISNS_HS_COMPUTING_N
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUIMVP_ISNS_P
	GROUP_DIFFPAIR1	GROUP1001_55G	GROUP1001	CPUIMVP_ISNS_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC1_VSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC1_VSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_VSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_VSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_ISENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_ISENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_ISENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ADC2_ISENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	SPKR_R_RSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	SPKR_R_RSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	SPKR_L_RSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	SPKR_L_RSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L01_L_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L01_L_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L01_R_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L01_R_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L02_L_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L02_L_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L02_R_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_L02_R_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_MIC_INL_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_MIC_INL_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_L1N_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_L1N_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_R1N_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_R1N_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_L0UBIN_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_L0UBIN_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_R0UBIN_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	AUD_SPKRAMP_R0UBIN_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	LSPKR_INTIV_RSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	LSPKR_INTIV_RSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	RSPKR_INTIV_RSENSE_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	RSPKR_INTIV_RSENSE_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	LSPKR_INTIV_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	LSPKR_INTIV_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	RSPKR_INTIV_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	RSPKR_INTIV_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ISNS_TBT_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ISNS_TBT_P
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ISNS_TBT_R_N
100%	AUDIO_DIFFPAIR1	AUDIO1001	AUDIO1001	ISNS_TBT_R_P

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	PCIE_CLK100M_AP	CLK_RCKR_80D	CLK_RCKR	PCIE_CLK100M_AP_CONN_P
	PCIE_CLK100M_80D	CLK_RCKR_80D	CLK_RCKR	PCIE_CLK100M_AP_CONN_N
	LT01_DIFFEAIR	LT01_DIFFEAIR		CHGR_CSI_R_P
	LT01_DIFFEAIR	LT01_DIFFEAIR		CHGR_CSI_R_N
	LT01_DIFFEAIR	LT01_DIFFEAIR		CHGR_CSO_R_P
	LT01_DIFFEAIR	LT01_DIFFEAIR		CHGR_CSO_R_N
	USB_EXTA	USB_ASD	USB	USB2_EXTA_MIXED_P
	USB_EXTA	USB_ASD	USB	USB2_EXTA_MIXED_N
	USB_EXTA	USB_ASD	USB	USB2_LTI_P
	USB_EXTA	USB_ASD	USB	USB2_LTI_N
		USB_ASD	USB	CONN_USB2_BT_P
		USB_ASD	USB	CONN_USB2_BT_N
		USB_ASD	USB	USB_LT2_P
		USB_ASD	USB	USB_LT2_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SSM2375SL_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SSM2375SL_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SSM2375SR_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	SSM2375SR_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SL_OUT_P_R
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SL_OUT_N_R
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SL_OUT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SL_OUT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSPKR_VSENSE_FILT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSPKR_VSENSE_FILT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSPKR_VSENSE_FILT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSPKR_VSENSE_FILT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SR_OUT_P_R
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SR_OUT_N_R
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SR_OUT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_SR_OUT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_L_OUT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_L_OUT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_R_OUT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_R_OUT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_S_OUT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SPKRCONN_S_OUT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSPKR_ISENSE_FILT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSPKR_ISENSE_FILT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSPKR_ISENSE_FILT_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSPKR_ISENSE_FILT_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSUBIN_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	RSUBIN_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSUBIN_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	LSUBIN_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SSM4321SR_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SSM4321SR_N
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SSM4321SL_P
	AUDIO_DIFFEAIR	DIFFEAIR	AUDIO	SSM4321SL_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_N
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_P
	AUDIO_DIFFEAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_N
		USB_ASD	USB	USB_TP4D_R_P
		USB_ASD	USB	USB_TP4D_R_N
		SB_POWER		PF3V3_S5
		SB_POWER		PF3V3_S0
		SB_POWER		PF1V5_S3RD0_CPHGR
		GND		GND

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		BRANCH	
		PAGE	108 OF 132
		SHEET	96 OF 99

8	7	6	5	4	3	2	1
15" MBP BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	16.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
8	7	6	5	4	3	2	1

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP, BOTTOM	0.058 MM	?
2:1_SPACING	TOP, BOTTOM	0.116 MM	?
3:1_SPACING	TOP, BOTTOM	0.174 MM	?
4:1_SPACING	TOP, BOTTOM	0.232 MM	?
5:1_SPACING	TOP, BOTTOM	0.290 MM	?
1:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
2:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.106 MM	?
3:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.159 MM	?
4:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.212 MM	?
5:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.265 MM	?
1:1_SPACING	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?
2:1_SPACING	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.202 MM	?
3:1_SPACING	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.303 MM	?
4:1_SPACING	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.404 MM	?
5:1_SPACING	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.505 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
2x_DIELECTRIC	TOP, BOTTOM	0.116 MM	?
3x_DIELECTRIC	TOP, BOTTOM	0.174 MM	?
4x_DIELECTRIC	TOP, BOTTOM	0.232 MM	?
5x_DIELECTRIC	TOP, BOTTOM	0.290 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
2x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.106 MM	?
3x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.159 MM	?
4x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.212 MM	?
5x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.265 MM	?
1x_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?
2x_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.202 MM	?
3x_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.303 MM	?
4x_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.404 MM	?
5x_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.505 MM	?

15" MBP Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING
AD01_1SENSE_P	AD01_1SENSE_P	
AD01_1SENSE_N	AD01_1SENSE_N	
CPUMVFP_1SNS1_P	CPUMVFP_1SNS1_P	46 65 66
CPUMVFP_1SNS1_N	CPUMVFP_1SNS1_N	46 66
CPUMVFP_1SNS20_P	CPUMVFP_1SNS20_P	46 66
CPUMVFP_1SNS20_N	CPUMVFP_1SNS20_N	46 66
CPUMVFP_1SNS2_P	CPUMVFP_1SNS2_P	46 65 66
CPUMVFP_1SNS2_N	CPUMVFP_1SNS2_N	46 66
CPUMVFP_1SNS3_P	CPUMVFP_1SNS3_P	46 65 66
CPUMVFP_1SNS3_N	CPUMVFP_1SNS3_N	46 66
CPUMVFP_1SUM_R_P	CPUMVFP_1SUM_R_P	46
CPUMVFP_1SUM_R_N	CPUMVFP_1SUM_R_N	46
CPUMVFP_1SUM3_R_P	CPUMVFP_1SUM3_R_P	46
CPUMVFP_1SUM3_R_N	CPUMVFP_1SUM3_R_N	46
GPXIMVP_1SNS1_P	GPXIMVP_1SNS1_P	80
GPXIMVP_1SNS1_N	GPXIMVP_1SNS1_N	80
GPXIMVP_1SNS2_P	GPXIMVP_1SNS2_P	80
GPXIMVP_1SNS2_N	GPXIMVP_1SNS2_N	80
ISNS_CPU_D0R_R_P	ISNS_CPU_D0R_R_P	98
ISNS_CPU_D0R_R_N	ISNS_CPU_D0R_R_N	98
ISNS_LCD_PANEL_P	ISNS_LCD_PANEL_P	
ISNS_LCD_PANEL_N	ISNS_LCD_PANEL_N	
ISNS_P1VSR1V15_CPUD0R_P	ISNS_P1VSR1V15_CPUD0R_P	
ISNS_P1VSR1V15_CPUD0R_N	ISNS_P1VSR1V15_CPUD0R_N	
ISNS_SSD_P	ISNS_SSD_P	39 99
ISNS_SSD_N	ISNS_SSD_N	39 99
ISNS_SSD_R_P	ISNS_SSD_R_P	99
ISNS_SSD_R_N	ISNS_SSD_R_N	99
PCHVCCIOSS_CS_P	PCHVCCIOSS_CS_P	87 99
PCHVCCIOSS_CS_N	PCHVCCIOSS_CS_N	87 99
PCH_VCCIOSENSE_P	PCH_VCCIOSENSE_P	87
PCH_VCCIOSENSE_N	PCH_VCCIOSENSE_N	87
GPUVCORE_SENSE_P	GPUVCORE_SENSE_P	79 80
GPUVCORE_SENSE_N	GPUVCORE_SENSE_N	79 80
GPU_FVIDDQ_SENSE	GPU_FVIDDQ_SENSE	73 74
GPU_FROND_SENSE	GPU_FROND_SENSE	73 74
P1V05_GPU_PEX_IOVDD_SNS_P	P1V05_GPU_PEX_IOVDD_SNS_P	74 79
P1V05_GPU_PEX_IOVDD_SNS_N	P1V05_GPU_PEX_IOVDD_SNS_N	74 79
SPKR1_THMNS_D2_P	SPKR1_THMNS_D2_P	
SPKR1_THMNS_D2_N	SPKR1_THMNS_D2_N	
SPKR_THMNS_D2_P	SPKR_THMNS_D2_P	
SPKR_THMNS_D2_N	SPKR_THMNS_D2_N	
TBT_THERMD_P	TBT_THERMD_P	47
TBT_THERMD_N	TBT_THERMD_N	47
X29THMNS_D2_P	X29THMNS_D2_P	
X29THMNS_D2_N	X29THMNS_D2_N	
VDDCI90_CS_P	VDDCI90_CS_P	
VDDCI90_CS_N	VDDCI90_CS_N	
GPXIMVP6_VSEN_P	GPXIMVP6_VSEN_P	
GPXIMVP6_VSEN_N	GPXIMVP6_VSEN_N	
USB3_EXTX_TX_F_P	USB3_EXTX_TX_F_P	
USB3_EXTX_TX_F_N	USB3_EXTX_TX_F_N	
USB3_EXTX_RX_F_P	USB3_EXTX_RX_F_P	
USB3_EXTX_RX_F_N	USB3_EXTX_RX_F_N	
USB3_EXTX_TX_C_P	USB3_EXTX_TX_C_P	40
USB3_EXTX_TX_C_N	USB3_EXTX_TX_C_N	40
USB3_EXTB_TX_C_P	USB3_EXTB_TX_C_P	7 38
USB3_EXTB_TX_C_N	USB3_EXTB_TX_C_N	7 38
USB3_EXTB_RX_RC_P	USB3_EXTB_RX_RC_P	38
USB3_EXTB_RX_RC_N	USB3_EXTB_RX_RC_N	38
USB3_EXTX_RX_RC_P	USB3_EXTX_RX_RC_P	40
USB3_EXTX_RX_RC_N	USB3_EXTX_RX_RC_N	40
P1V5_GPU_VSNS	P1V5_GPU_VSNS	
P1V05_VSNS	P1V05_VSNS	

PCB Rule Definitions

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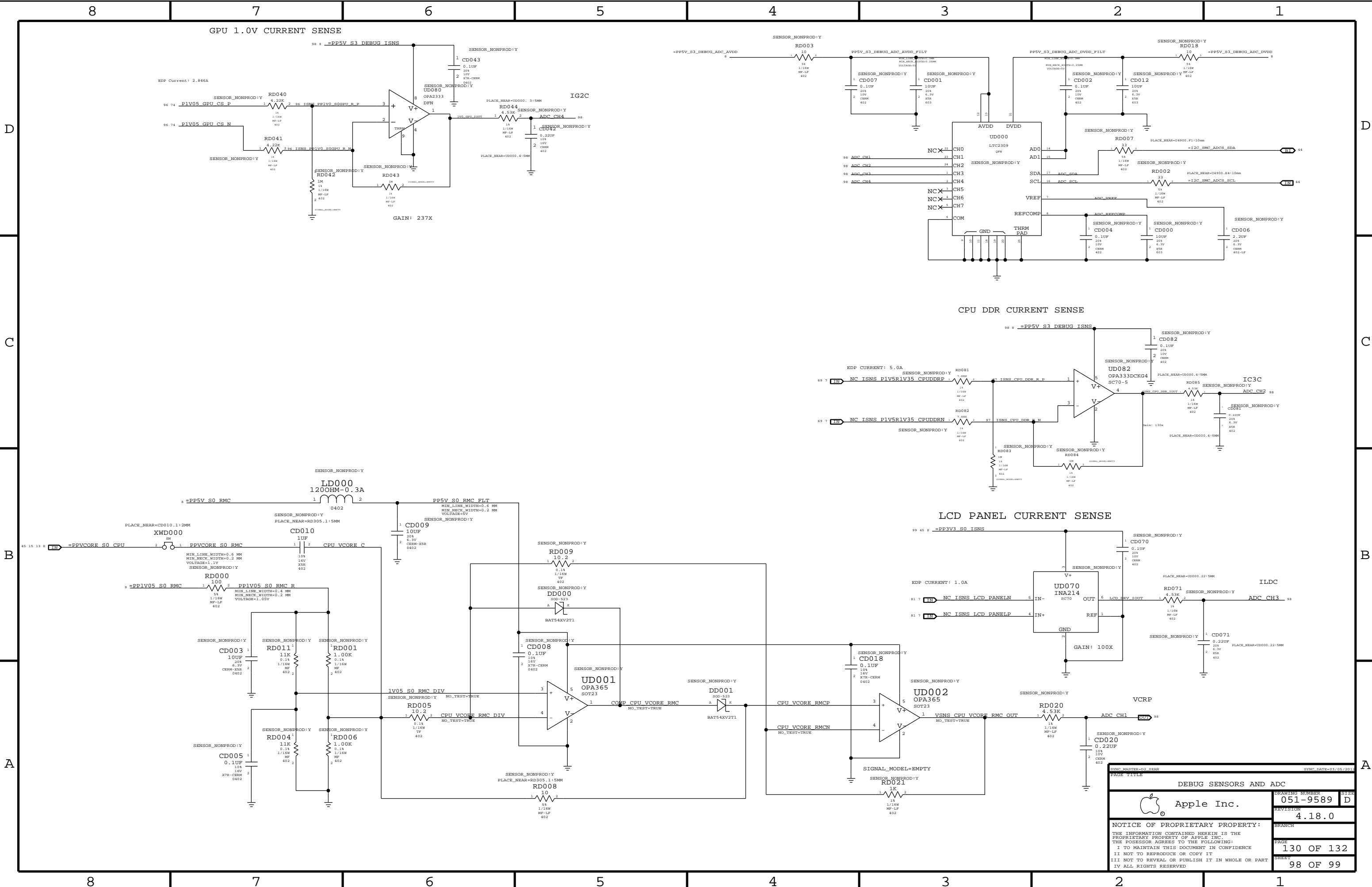
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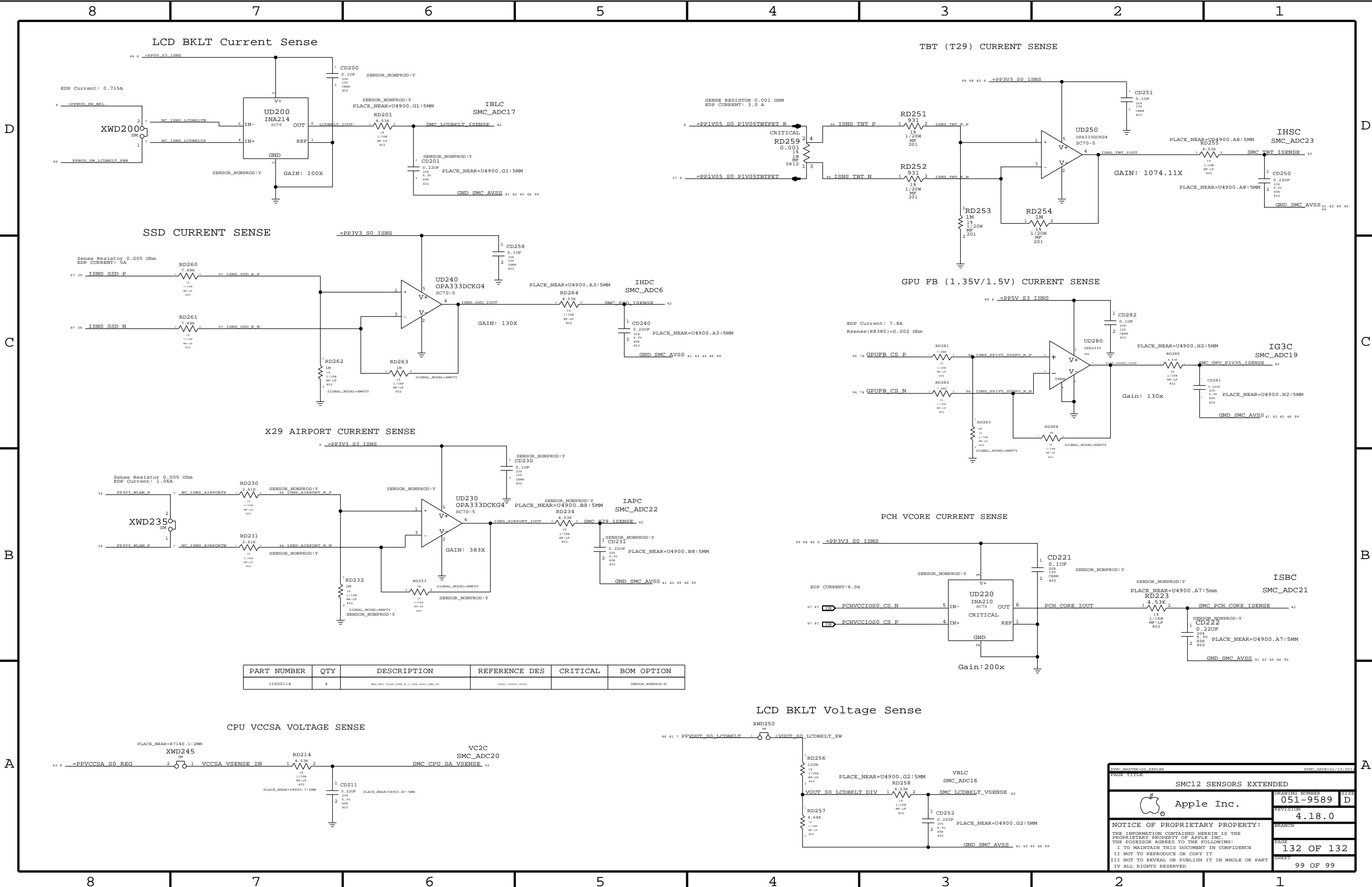
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109 OF 132

97 OF 99



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	PAGE	130 OF 132
	SHEET	98 OF 99




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PAGE
132 OF 132
SHEET
99 OF 99

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